10-100MHz 10/12- Bit DC-Balanced FPD-Link III Serializer and Deserializer with Bidirectional Control Channel

General Description

The DS90UB913Q/DS90UB914Q chipset offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single differential pair. The DS90UB913Q/914Q chipsets incorporate differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The Serializer/ Deserializer pair is targeted for connections between imagers and video processors in an ECU (Electronic Control Unit). This chipset is ideally suited for driving video data requiring up to 12 bit pixel depth plus two synchronization signals along with bidirectional control channel bus.

There is a multiplexer at the Deserializer to choose between two input imagers. The Deserializer can have only one active input imager. The primary video transport converts 10/12 bit data over a single high-speed serial stream, along with a separate low latency bidirectional control channel transport that accepts control information from an I2C port and is independent of video blanking period.

Using TI's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical bidirectional control channel information in both directions. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins. In addition, the Deserializer inputs provide adaptive equalization to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects. The Serializer is offered in a 32-pin LLP package and the Deserializer is offered in a 48-pin LLP package.

Features

- 10 MHz to 100 MHz input pixel clock support
- Single differential pair interconnect
- Programmable data payload:
  - 10 bit payload up to 100Mhz
  - 12 bit payload up to 75MHz
- Continuous Low Latency Bidirectional control interface channel with I²C support@400kHz
- 2:1 Multiplexer to choose between two input imagers
- Embedded clock with DC Balanced coding to support AC-coupled interconnects
- Capable of driving up to 25 meters shielded twisted-pair
- Receive Equalizer automatically adapts for changes in cable loss
- 4 dedicated General Purpose Input (GPI)/ Output (GPO)
- LOCK output reporting pin and AT-SPEED BIST diagnosis feature to validate link integrity
- 1.8V, 2.8V or 3.3V compatible parallel inputs on Serializer
- Single power supply at 1.8V
- ISO 10605 and IEC 61000-4-2 ESD Compliant
- Automotive grade product: AEC-Q100 Grade 2 qualified
- Temperature range –40°C to +105°C
- Small serializer footprint (5mm x 5mm)
- EMI/EMC Mitigation - Deserializer
  - Programmable Spread Spectrum (SSCG) outputs.
  - Receiver staggered outputs

Applications

- Front or rear view camera for collision mitigation
- Surround view for parking assistance

Typical Application Diagram

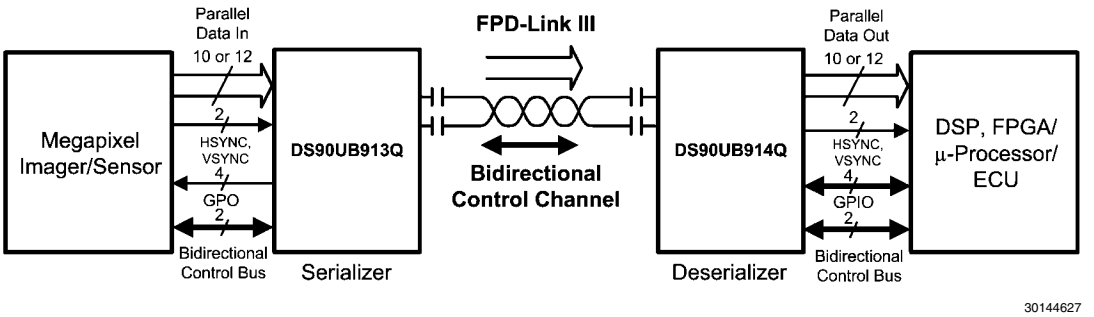

FIGURE 1. Typical Application Circuit

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Block Diagrams

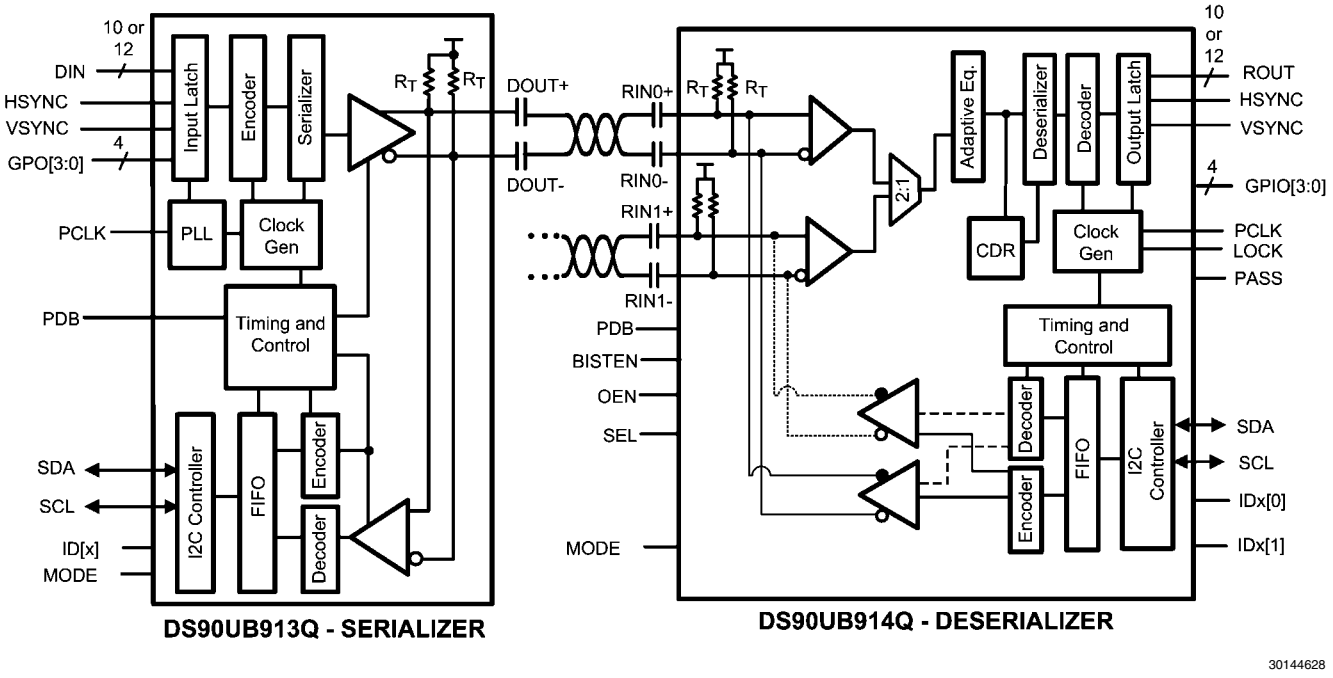


FIGURE 2. Block Diagram

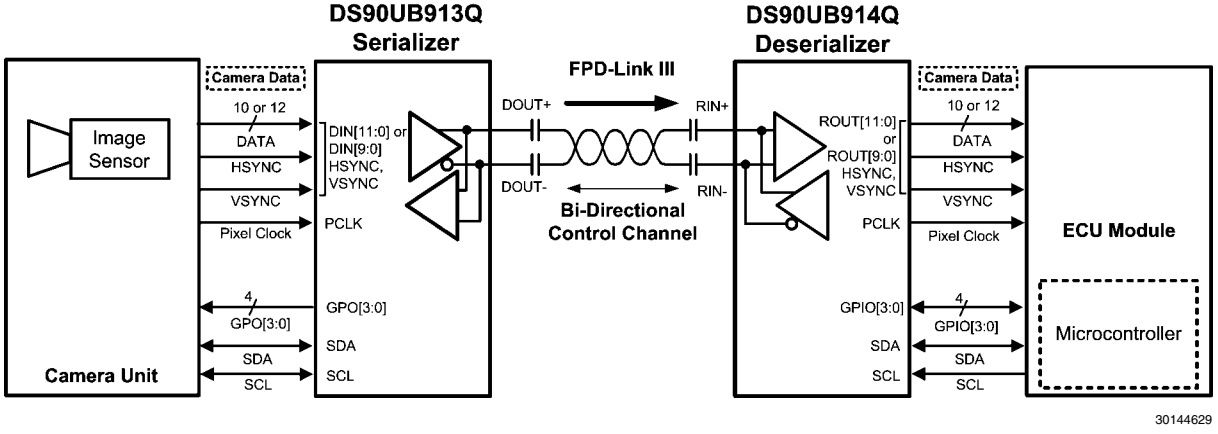
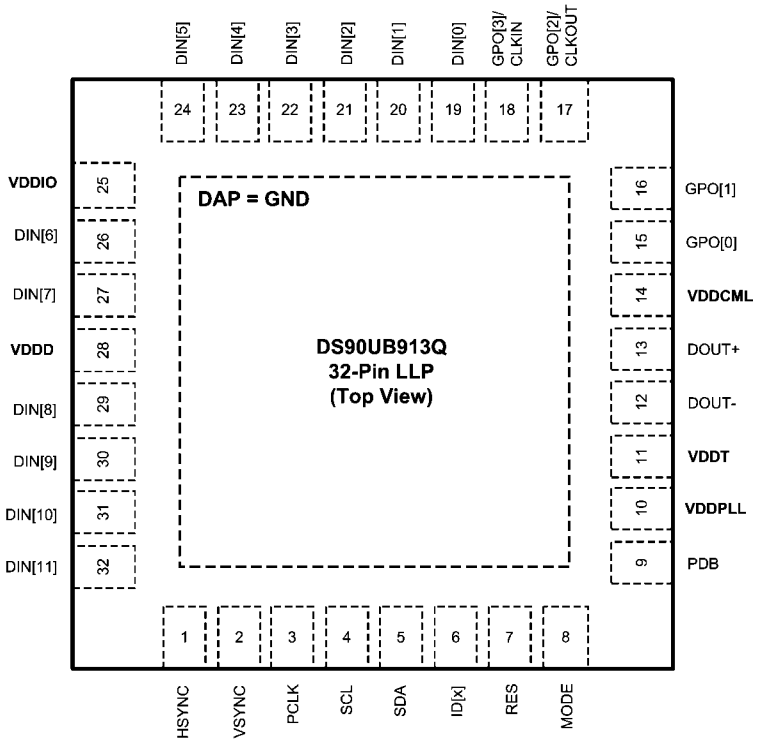


FIGURE 3. Application Block Diagram

Ordering Information

NSID	Package Description	Quantity	SPEC	Package ID
DS90UB913QSQE	32-pin LLP, 5.0 X 5.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA32A
DS90UB913QSQ	32-pin LLP, 5.0 X 5.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA32A
DS90UB913QSQX	32-pin LLP, 5.0 X 5.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA32A
DS90UB914QSQE	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS90UB914QSQ	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS90UB914QSQX	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA48A

DS90UB913Q Pin Diagram



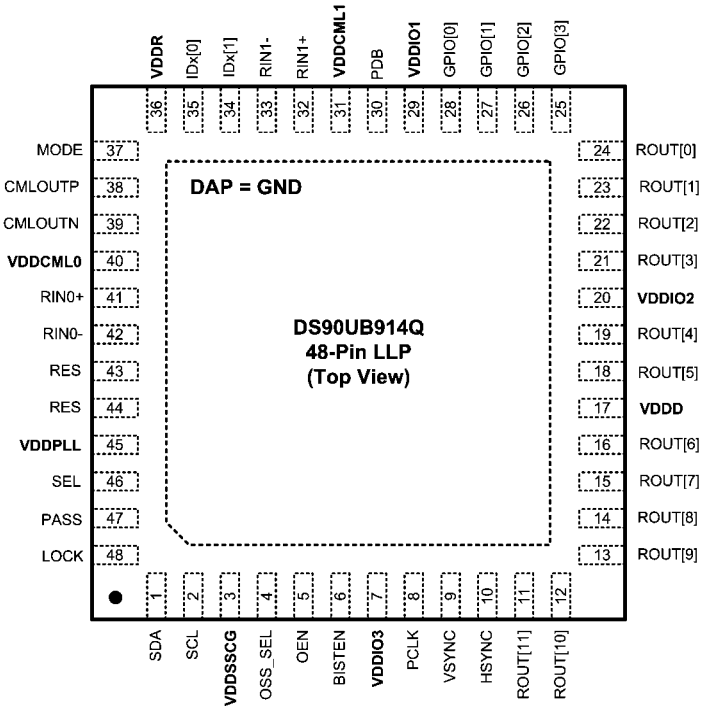
Serializer - DS90UB913Q — Top View

DS90UB913Q Serializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
DIN[0:11]	19,20,21,22, 23,24,26,27, 29,30,31,32	Inputs, LVCMOS w/ pull down	Parallel Data Inputs.
HSYNC	1	Inputs, LVCMOS w/ pull down	Horizontal SYNC Input
VSYNC	2	Inputs, LVCMOS w/ pull down	Vertical SYNC Input
PCLK	3	Input, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by TRFB control register.
GENERAL PURPOSE OUTPUT (GPO)			

Pin Name	Pin No.	I/O, Type	Description
GPO[1:0]	16,15	Output, LVCMOS	General-purpose output pins can be configured as outputs; used to control and respond to various commands. GPO[0:1] can be configured to be the outputs for input signals coming from GPIO[0:1] pins on the Deserializer or can be configured to be outputs of the local register on the Serializer.
GPO[2]/ CLKOUT	17	Output, LVCMOS	GPO2 pin can be configured to be the output for input signal coming from the GPIO2 pin on the Deserializer or can be configured to be the output of the local register on the Serializer. It can also be configured to be the output clock pin when the DS90UB913Q device is used in the External Oscillator mode. See Applications Information for a detailed description of the DS90UB913/914Q chipsets working with the external oscillator.
GPO[3]/CLKIN	18	Input/Output, LVCMOS	GPO3 can be configured to be the output for input signals coming from the GPIO3 pin on the Deserializer or can be configured to be the output of the local register setting on the Serializer. It can also be configured to be the input clock pin when the DS90UB913Q Serializer is working with an external oscillator. See Applications Information section for a detailed description of the DS90UB913/914Q chipsets working with an external oscillator.
BIDIRECTIONAL CONTROL BUS - I²C COMPATIBLE			
SCL	4	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	5	Input/Output, Open Drain	Data line for the bidirectional control bus communication SDA requires an external pull-up resistor to V_{DDIO}.
MODE	8	Input, LVCMOS w/ pull down	**Device mode select** Resistor to Ground and 10 kΩ pull-up to 1.8V rail. MODE pin on the Serializer can be used to select whether the system is running off the PCLK from the imager or an external oscillator. See details in *Table 5*
ID[x]	6	Input, analog	**Device ID Address Select** The ID[x] pin on the Serializer is used to assign the I2C device address. Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 7*
CONTROL AND CONFIGURATION			
PDB	9	Input, LVCMOS w/ pull down	**Power down Mode Input Pin.** PDB = H, Serializer is enabled and is ON. PDB = L, Serailizer is in Power Down mode. When the Serializer is in Power Down, the PLL is shutdown, and IDD is minimized. Programmed control register data are NOT retained and reset to default values
RES	7	Input, LVCMOS w/ pull down	Reserved. **This pin MUST be tied LOW.**
FPD–Link III INTERFACE			
DOUT+	13	Input/Output, CML	Non-inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 100 nF capacitor.
DOUT-	12	Input/Output, CML	Inverting differential output, bidirectional control channel input. The interconnect must be AC Coupled with a 100 nF capacitor.
POWER AND GROUND			
VDDPLL	10	Power, Analog	PLL Power, 1.8V ±5%
VDDT	11	Power, Analog	Tx Analog Power, 1.8V ±5%
VDDCML	14	Power, Analog	CML & Bidirectional Channel Driver Power, 1.8V ±5%
VDDD	28	Power, Digital	Digital Power, 1.8V ±5%
VDDIO	25	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 2.8±10% or 3.3V ±10%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the LLP package. Connected to the ground plane (GND) with at least 9 vias.

DS90UB914Q Pin Diagram



Deserializer - DS90UB914Q — Top View

DS90UB914Q Deserializer Pin Descriptions

Pin Name	Pin No.	I/O, Type	Description
LVCMOS PARALLEL INTERFACE			
ROUT[11:0]	11,12,13,14, 15,16,18,19, 21,22,23,24	Outputs, LVCMOS	Parallel Data Outputs.
HSYNC	10	Output, LVCMOS	Horizontal SYNC Output.
VSYNC	9	Output, LVCMOS	Vertical SYNC Output.
PCLK	8	Output, LVCMOS	Pixel Clock Output Pin. Strobe edge set by RRFB control register.
GENERAL PURPOSE INPUT/OUTPUT (GPIO)			
GPI0[1:0]	27,28	Digital Input/ Output, LVCMOS	General-purpose input/output pins can be used to control and respond to various commands. They may be configured to be the input signals for the corresponding GPOs on the serializer or they may be configured to be outputs to follow local register settings.
GPIO[3:2]	25,26	Digital Input/ Output LVCMOS	General purpose input/output pins GPO[2:3] can be configured to be input signals for GPOs on the Serializer. In addition they can also be configured to be outputs to follow the local register settings. When the SerDes chipsets are working with an external oscillator, these pins can be configured only to be outputs to follow the local register settings.
BIDIRECTIONAL CONTROL BUS - I²C COMPATIBLE			
SCL	2	Input/Output, Open Drain	Clock line for the bidirectional control bus communication SCL requires an external pull-up resistor to V_{DDIO}.
SDA	1	Input/Output, Open Drain	Data line for bidirectional control bus communication SDA requires an external pull-up resistor to V_{DDIO}.

Pin Name	Pin No.	I/O, Type	Description
MODE	37	Input, LVCMOS w/ pull up	**Device mode select pin** Resistor to Ground and 10 kΩ pull-up to 1.8V rail. The MODE pin on the Deserializer can be used to configure the Serializer and Deserializer to work in different input PCLK range. See details in Table 2. **12– bit low frequency mode – (10- 50 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 12 bits DATA+2 SYNC. Input PCLK range is from 10MHz to 50MHz. **12– bit high frequency mode – (15-75 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 12 bits DATA + 2 SYNC. Input PCLK range is from 15MHz to 75MHz. **10–bit mode– (20–100 MHz operation):** In this mode, the Serializer and Deserializer can accept up to 10 bits DATA + 2 SYNC. Input PCLK frequency can range from20 MHz to 100MHz. Please refer to *Table 6* in the Applications Information section on how to configure the MODE pin on the Deserializer.
IDx[0:1]	35,34	Input, analog	The IDx[0] and IDx[1] pins on the Deserializer are used to assign the I2C device address. Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See *Table 8*
CONTROL AND CONFIGURATION			
PDB	30	Input, LVCMOS w/ pull down	**Power down Mode Input Pin.** PDB = H, Deserializer is enabled and is ON. PDB = L, Deserializer is in Sleep (power down mode). When the Deserializer is in Sleep, programmed control register data are NOT retained and reset to default values.
LOCK	48	Output, LVCMOS	**LOCK Status Output Pin.** LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL control register. May be used as Link Status.
BISTEN	6	Input LVCMOS w/ pulldown	**BIST Enable pin** **BISTEN=H**, BIST Mode Enabled **BISTEN=L**, BIST Mode is disabled
PASS	47	Output, LVCOMS	**PASS Output Pin for BIST mode.** **PASS = H**, ERROR FREE Transmission **PASS = L**, one or more errors were detected in the received payload. See BIST section for more information. Leave Open if unused. Route to test point (pad) recommended.
OEN	5	Input LVCMOS w/ pulldown	Output Enable Input Refer to *Table 9*
OSS_SEL	4	Input LVCMOS w/ pulldown	Output Sleep State Select Pin Refer to *Table 9*
SEL	46	Input LVCMOS w/ pulldown	MUX Select line **SEL = L**, RIN0+/- input. This selects input A as the active channel on the Deserializer. **SEL = H**, RIN1+/- input. This selects input B as the active channel on the Deserializer.
FPD–Link III INTERFACE			
RIN0+	41	Input/Output, CML	Non-Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 100 nF capacitor
RIN0-	42	Input/Output, CML	Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 100 nF capacitor
RIN1+	32	Input/Output, CML	Non-Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 100 nF capacitor
RIN1-	33	Input/Output, CML	Inverting Differential input, bidirectional control channel. The IO must be AC coupled with a 100 nF capacitor

Pin Name	Pin No.	I/O, Type	Description
RES	43,44	—	Reserved. **This pin must always be tied low**
CMLOUTP/N	38,39		Route to test point or leave open if unused
POWER AND GROUND			
VDDIO1/2/3	29, 20, 7	Power, Digital	LVCMOS I/O Buffer Power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10%
VDDD	17	Power, Digital	Digital Core Power, 1.8V ±5%
VDDSSCG	3	Power, Analog	SSCG PLL Power, 1.8V ±5%
VDDR	36	Power, Analog	Rx Analog Power, 1.8V ±5%
VDDCML0/1	40,31	Power, Analog	CML and Bidirectional control channel Drive Power, 1.8V±5%
VDDPLL	45	Power, Analog	PLL Power, 1.8V ±5%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the LLP package. Connected to the ground plane (GND) with at least 16 vias.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS Input Voltage I/O Voltage	−0.3V to + (VDDIO + 0.3V)
CML Driver I/O Voltage (V_{DD})	−0.3V to +(V_{DD} + 0.3V)
CML Receiver I/O Voltage (V_{DD})	−0.3V to (V_{DD} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Maximum Package Power Dissipation Capacity Package	1/θ_{JA} °C/W above +25°
Package Derating: DS90UB913Q 32L LLP	
θ_{JA} *(based on 16 thermal vias)*	38.4 °C/W
θ_{JC} *(based on 16 thermal vias)*	6.9 °C/W
DS90UB914Q 48L LLP	
θ_{JA} *(based on 16 thermal vias)*	26.9 °C/W
θ_{JC} *(based on 16 thermal vias)*	4.4 °C/W
ESD Rating (IEC 61000-4-2)	R_D = 330Ω, C_S = 150pF
Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±25 kV
Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±7 kV
ESD Rating (ISO10605)	R_D = 330Ω, C_S = 150/330pF
ESD Rating (ISO10605)	R_D = 2KΩ, C_S = 150/330pF
Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±15 kV
Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1 kV
ESD Rating (MM)	≥±250 V

For soldering specifications:
see product folder at www.ti.com and
www.ti.com/lit/an/snoa549c/snoa549c.pdf

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) OR	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) OR	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO}) Only Serializer	2.52	2.8	3.08	V
Supply Noise				

	Min	Nom	Max	Units
V_{DDn} (1.8V)			25	mVp-p
V_{DDIO} (1.8V)			25	mVp-p
V_{DDIO} (3.3V)			50	mVp-p
Operating Free Air Temperature (T_A)	-40	+25	+105	°C
PCLK Clock Frequency	10		100	MHz

Electrical Characteristics (*Note 2*, *Note 3*, *Note 4*)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS 3.3V I/O (SER INPUTS, DES OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3.0V to 3.6V		2.0		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3.0V to 3.6V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V V_{IN} = 3.0V to 3.6V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = –4 mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OL} = +4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-15		mA
			Deserializer LVCMOS Outputs		-35		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (SER INPUTS, DES OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71V to 1.89V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71V to 1.89V		GND		0.35 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{IN} = 1.71V to 1.89V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = –4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OL} = +4 mA	Deserializer LVCMOS Outputs	GND		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-11		mA
			Deserializer LVCMOS Outputs		-17		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
LVCMOS DC SPECIFICATIONS 2.8V I/O (SER INPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 2.52V to 3.08V		0.7 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 2.52V to 3.08V		GND		0.3 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 3.08V V_{IN} = 2.52V to 3.08V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 2.52V to 3.08V I_{OH} = –4 mA		V_{DDIO} - 0.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} =2.52V to 3.08V I_{OL} = +4 mA	Deserializer LVCMOS Outputs	GND		0.4	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-11		mA
			Deserializer LVCMOS Outputs		-20		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100Ω (*Figure 7*)		268	340	412	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω			1	50	mV
V_{OS}	Output Differential Offset Voltage	R_L = 100Ω (*Figure 7*)			V_{DD} - $V_{OD/2}$		V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V			-26		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT-		80	100	120	Ω
CML RECEIVER DC SPECIFICATIONS (RIN0+,RIN0–,RIN1+,RIN1–)							
I_{IN}	Input Current	V_{IN} = V_{DD} or 0V, V_{DD} = 1.89V		-20	1	+20	µA
R_T	Differential Internal Termination Resistance	Differential across RIN+ and RIN-		80	100	120	Ω
CML RECEIVER AC SPECIFICATIONS (RIN0+,RIN0–,RIN1+,RIN1–)							
$\|V_{swing}\|$	Minimum allowable swing for 1010 pattern (*Note 10*)	Line Rate = 1.4Gbps (*Figure 8*)		135			mV
CMLMONITOR OUTPUT DRIVER SPECIFICATIONS(CMLOUTP, CMLOUTN)							
E_w	Differntial Output Eye Opening	R_L = 100Ω Jitter Frequency>f/40 (*Figure 17*)			0.45		UI
E_H	Differential Output Eye Height				200		mV
SER/DES SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDD							

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDT}	Serializer (Tx) V_{DDn} Supply Current (includes load current)	R_L = 100Ω WORST CASE pattern (*Figure 5*)	VDDn=1.89V VDDIO=3.6V f = 100 MHz, 10 bit mode Default Registers		61	80	mA
			VDDn=1.89V VDDIO=3.6V f = 75 MHz, 12 bit high frequency mode Default Registers		61	80	mA
			VDDn=1.89V VDDIO=3.6V f = 50 MHz, 12 bit low frequency mode Default Registers		61	80	
		R_L = 100Ω RANDOM PRBS-7 pattern	VDDn=1.89V VDDIO=3.6V f = 100 MHz, 10 bit mode Default Registers		54		mA
			VDDn=1.89V VDDIO=3.6V f = 75 MHz, 12 bit high frequency mode Default Registers		54		
			VDD=1.89V VDDIO=3.6V f = 50 MHz, 12 bit low frequency mode Default Registers		54		
I_{DDIOT}	Serializer (Tx) VDDIO Supply Current (includes load current)	R_L = 100Ω WORST CASE pattern (*Figure 5*)	VDDIO=1.89V f = 75 MHz, 12 bit high frequency mode Default Registers		1.5	3	mA
			VDDIO=3.6V f = 75 MHz, 12 bit high frequency mode Default Registers		5	8	
I_{DDTZ}	Serializer (Tx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	VDDIO=1.89V Default Registers		300	900	µA
			VDDIO=3.6V Default Registers		300	900	µA
I_{DDIOTZ}	Serializer (Tx) VDDIO Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	VDDIO=1.89V Default Registers		15	100	µA
			VDDIO=3.6V Default Registers		15	100	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDIOR}	Deserializer (Rx) Total Supply Current (includes load current)	V_{DDIO}=1.89V C_L=8pF Worst Case Pattern	f=100MHz, 10–bit mode		22	42	mA
			f=75MHz, 12–bit high freq mode		19	39	
			f=50MHz, 12–bit low freq mode		21	32	
		V_{DDIO}=1.89V C_L=8pF Random Pattern	f=100MHz, 10–bit mode		15		mA
			f=75MHz, 12–bit high freq mode		12		
			f=50MHz, 12–bit low freq mode		14		
		V_{DDIO}=3.6V C_L=8pF Worst Case Pattern	f=100MHz, 10–bit mode		42	55	mA
			f=75MHz, 12–bit high freq mode		37	50	
			f=50MHz, 12–bit low freq mode		25	38	
		V_{DDIO}=3.6V C_L=8pF Random Pattern	f=100MHz, 10–bit mode		35		mA
			f=75MHz, 12–bit high freq mode		30		
			f=50MHz, 12–bit low freq mode		18		
		V_{DDIO}=1.89V C_L=4pF Worst Case Pattern	f=100MHz, 10–bit mode		15		mA
			f=75MHz, 12–bit high freq mode		11		
			f=50MHz, 12–bit low freq mode		16		
		V_{DDIO}=1.89V C_L=4pF Random Pattern	f=100MHz, 10–bit mode		8		mA
			f=75MHz, 12–bit high freq mode		4		
			f=50MHz, 12–bit low freq mode		9		
		V_{DDIO}=3.6V C_L=4pF Worst Case Pattern	f=100MHz, 10–bit mode		36		mA
			f=75MHz, 12–bit high freq mode		29		
			f=50MHz, 12–bit low freq mode		20		
		V_{DDIO}=3.6V C_L=4pF Random Pattern	f=100MHz, 10–bit mode		29		mA
			f=75MHz, 12–bit high freq mode		22		
			f=50MHz, 12–bit low freq mode		13		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{DDR}	Deserializer (Rx) VDDn Supply Current (includes load current)	V_{DDn}=1.89V C_L=4pF Worst Case Pattern	f=100MHz, 10–bit mode		64	110	mA
			f=75MHz, 12–bit high freq mode		67	114	
			f=50MHz, 12–bit low freq mode		63	96	
		V_{DDn}=1.89V C_L=4pF Random Pattern	f=100MHz, 10–bit mode		57		
			f=75MHz, 12–bit high freq mode		60		
			f=50MHz, 12–bit low freq mode		56		
I_{DDRZ}	Deserializer (Rx) Supply Current Power-down	PBB=0V All other LVCMOS Inputs=0V	VDDIO=1.89V Default Registers		42	400	µA
		PBB=0V All other LVCMOS Inputs=0V	VDDIO=3.6V Default Registers		42	400	
I_{DDIORZ}	Deserializer (Rx) VDD Supply Current Power-down	PDB = 0V All other LVCMOS Inputs = 0V	V_{DDIO} = 1.89V		8	40	µA
			V_{DDIO} = 3.6V		360	800	

Recommended Serializer Timing for PCLK (*Note 12*)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	10–bit Mode		10	T	50	ns
		12–bit high frequency mode		13.33	T	66.66	ns
		12–bit low frequency mode		20	T	100	ns
t_{TCIH}	Transmit Clock Input High Time			0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Input Low Time			0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK Input Transition Time (*Figure 9*)	20MHz–100 MHz, 10 bit mode		0.5T	2.5T	0.3T	ns
		15MHz -75MHz, 12 bit high frequency mode		0.5T	2.5T	0.3T	ns
		10MHz-50MHz, 12 bit low frequency mode		0.5T	2.5T	0.3T	ns
t_{JIT0}	PCLK Input Jitter (PCLK from imager mode)	Refer to Jitter freq>f/40	f=10–100MHz		0.1T		ns
t_{JIT1}	PCLK Input Jitter (External Oscillator mode)	Refer to Jitter freq>f/40	f=10–100MHz		1T		ns
t_{JIT2}	External Oscillator Jitter				0.1		UI

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	CML Low-to-High Transition Time	R_L = 100Ω (*Figure 6*)		150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100Ω (*Figure 6*)		150	330	ps
t_{DIS}	Data Input Setup to PCLK	Serializer Data Inputs (*Figure 10*)	2			ns
t_{DIH}	Data Input Hold from PCLK		2			ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω (*Note 5*, *Note 11*), (*Figure 11*)		1	2	ms
t_{SD}	Serializer Delay (*Note 11*)	R_T = 100Ω 10–bit mode Register 0x03h b[0] (TRFB = 1) (*Figure 12*)	32.5T	38T	44T	ns
		R_T = 100Ω 12–bit mode Register 0x03h b[0] (TRFB = 1) (*Figure 12*)	11.75T	13T	15T	ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter . Measured (cycle-cycle) with PRBS-7 test pattern (*Note 4*, *Note 13*)		0.13		UI
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern. (*Note 4*, *Note 13*)		0.04		UI
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measured (cycle-cycle) with PRBS-7 test pattern. (*Note 4*, *Note 13*)		0.396		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth (*Note 10*)	PCLK = 100MHz 10–bit mode. Default Registers		2.2		MHz
		PCLK = 75MHz 12–bit high frequency mode. Default Registers		2.2		
		PCLK = 50MHz 12–bit low frequency mode. Default Registers		2.2		
δ_{STX}	Serializer Jitter Transfer Function (Peaking) (*Note 10*)	PCLK = 100MHz 10–bit mode. Default Registers		1.06		dB
		PCLK = 75MHz 12–bit high frequency mode. Default Registers		1.09		
		PCLK = 50MHz 12–bit low frequency mode. Default Registers		1.16		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency) (*Note 10*)	PCLK = 100MHz 10–bit mode. Default Registers		400		kHz
		PCLK = 75MHz 12–bit high frequency mode. Default Registers		500		
		PCLK = 50MHz 12–bit low frequency mode. Default Registers		600		

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver Output Clock Period	10–bit mode	PCLK (*Figure 16*)	10		50	ns
		12–bit high frequency mode		13.33		66.66	
		12–bit low frequency mode		10		100	
t_{PDC}	PCLK Duty Cycle	10–bit mode	PCLK	45	50	55	%
		12–bit high frequency mode		40	50	60	
		12–bit low frequency mode		40	50	60	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 14*), (*Note 10*)	PCLK	1.3	2	2.8	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1.3	2	2.8	
t_{CLH}	LVCMOS Low-to-High Transition Time	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 14*) ,(*Note 10*)	ROUT[11:0], HS, VS	1	2.5	4	ns
t_{CHL}	LVCMOS High-to-Low Transition Time			1	2.5	4	
t_{ROS}	ROUT Setup Data to PCLK	V_{DDIO}: 1.71V to 1.89V or 3.0V to 3.6V, C_L = 8 pF (lumped load) Default Registers (*Figure 16*)	ROUT[11:0], HS, VS	0.38T	0.5T		ns
t_{ROH}	ROUT Hold Data to PCLK			0.38T	0.5T		
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) (*Figure 15*),(*Note 10*)	10–bit mode	154T		158T	ns
			12–bit low frequency mode	109T		112T	
			12–bit high frequency mode	73T		75T	
t_{DDLT}	Deserializer Data Lock Time	With Adaptive Equalization (*Figure 13*)	10–bit mode		15	22	ms
			12–bit low frequency mode		15	22	
			12–bit high frequency mode		15	22	
t_{RCJ}	Receiver Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 10*)	10–bit mode PCLK=100MHz		20	30	ps
			12–bit low frequency mode PCLK=50MHz		22	35	
			12–bit high frequency mode PCLK=75MHz		45	90	
t_{DPJ}	Deserializer Period Jitter	PCLK SSCG[3:0] = OFF (*Note 7*, *Note 10*)	10–bit mode PCLK=100MHz		170	815	ps
			12–bit low frequency mode PCLK=50MHz		180	330	
			12–bit high frequency mode PCLK=75MHz		300	515	

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DCCJ}	Deserializer Cycle-to-Cycle Clock Jitter	PCLK SSCG[3:0] = OFF (*Note 8*, *Note 10*)	10–bit mode PCLK=100MHz		440	1760	ps
			12–bit low frequency mode PCLK=50MHz		460	730	
			12–bit high frequency mode PCLK=75MHz		565	985	
fdev	Spread Spectrum Clocking Deviation Frequency	LVCMOS Output Bus SSC[3:0] = ON (*Figure 21*),(*Note 10*)	10 MHz–100 MHz		±0.5 to ±1.5		%
fmod	Spread Spectrum Clocking Modulation Frequency		10 MHz–100 MHz		5 to 50		kHz

AC Timing Specifications (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified.(*Figure 4*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
f_{SCL}	SCL Clock Frequency	Standard Mode	>0		100	kHz
		Fast Mode	>0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free time between Stop and Start	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

Bidirectional Control Bus DC Timing Specifications (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
V_{IH}	Input High Level	SDA and SCL	$0.7*V_{DDIO}$		V_{DDIO}	V
V_{IL}	Input Low Level	SDA and SCL	GND		$0.3*V_{DDIO}$	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level	SDA, I_{OL}=0.5mA	0		0.4	V
I_{IN}	Input Current	SDA or SCL, $V_{IN}=V_{DDOP}$ OR GND	—10		10	µA
t_R	SDA Rise Time-READ	SDA, RPU = 10kΩ, Cb ≤ 400pF (*Figure 4*)		430		ns
t_F	SDA Fall Time-READ			20		ns
$t_{SU;DAT}$		(*Figure 4*)		560		ns
$t_{HD;DAT}$		(*Figure 4*)		615		ns
t_{SP}				50		ns
C_{IN}		SDA or SCL		<5		pF

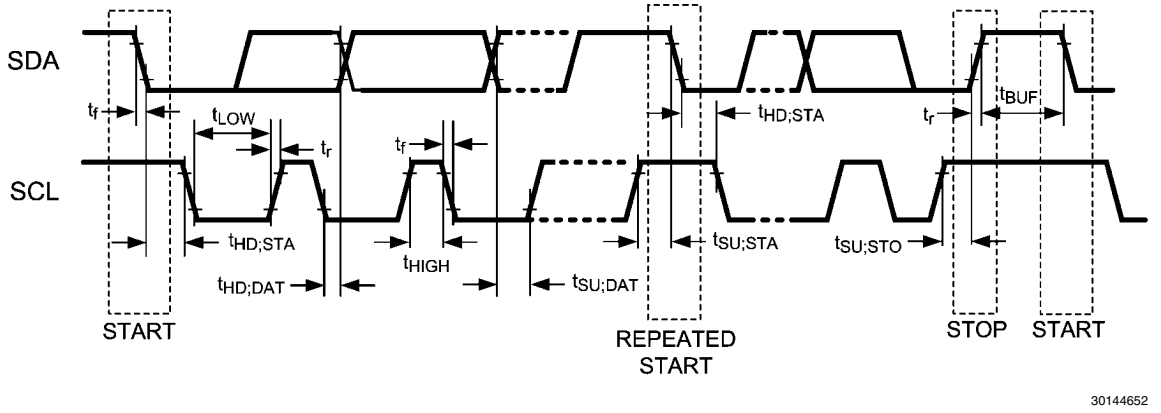


FIGURE 4. Bi-directional Control Bus Timing

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 5: t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK

Note 6: t_{DCJ} is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).

Note 7: t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.

Note 8: t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

Note 9: Supply noise testing was done with minimum capacitors (as shown on Figures 42, 44) on the PCB. A sinusoidal signal is AC coupled to the VDDn (1.8V) supply with amplitude = 25 mVp-p measured at the device VDDn pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

Note 10: Specification is guaranteed by characterization and is not tested in production.

Note 11: Specification is guaranteed by design.

Note 12: Recommended Input Timing Requirements are input specifications and not tested in production.

Note 13: UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.

Note 14: t_{RJIT} max (0.61UI) is limited by instrumentation and actual t_{RJIT} of in-band jitter at low frequency (<2 MHz) is greater 1 UI.

AC Timing Diagrams and Test Circuits

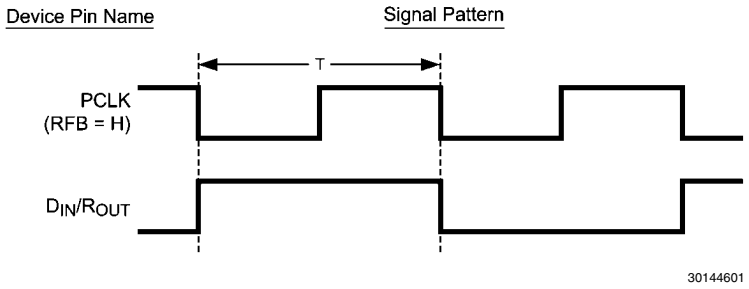
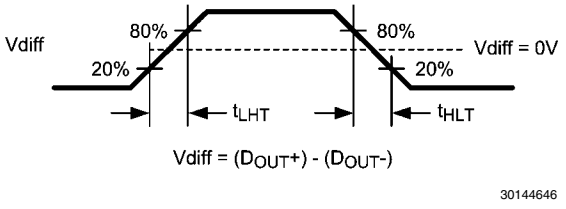


FIGURE 5. "Worst Case" Test Pattern



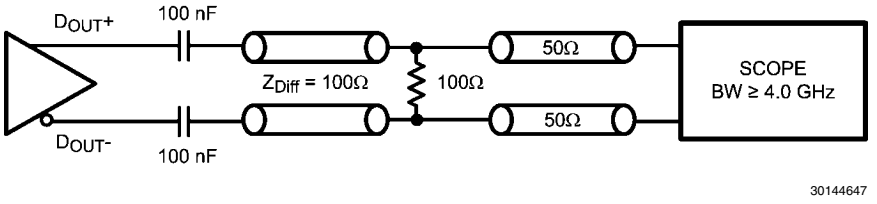
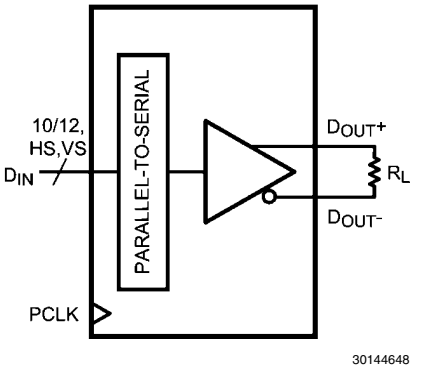


FIGURE 6. Serializer CML Output Load and Transition Times



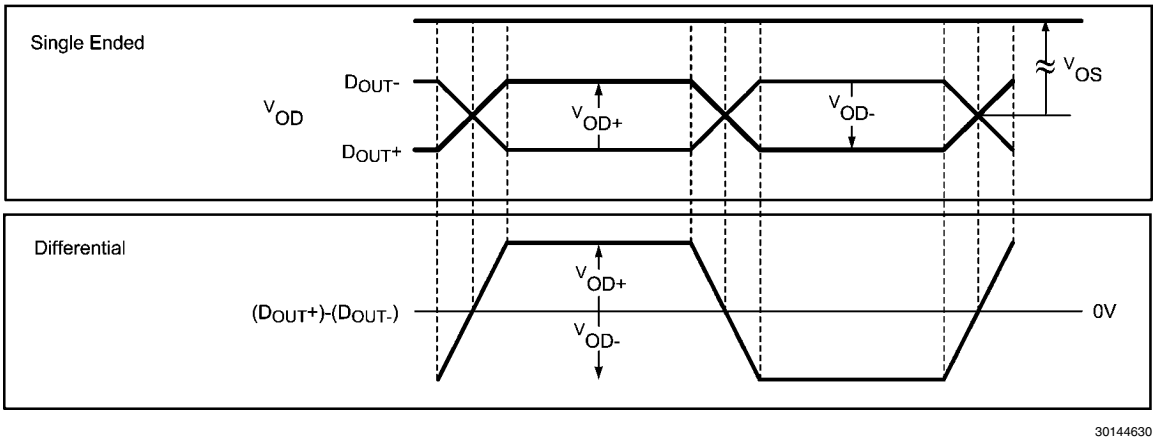


FIGURE 7. Serializer VOD Diagram

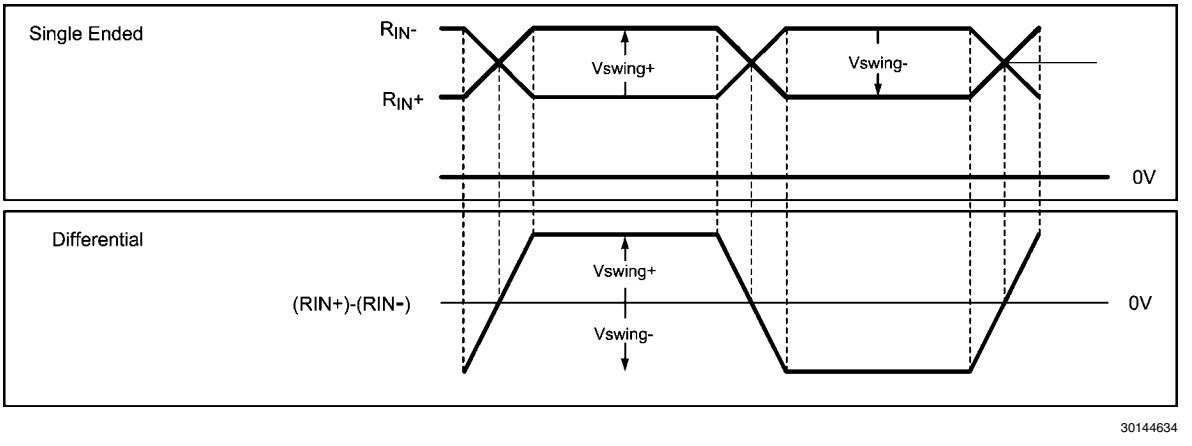


FIGURE 8. Differential Vswing Diagram

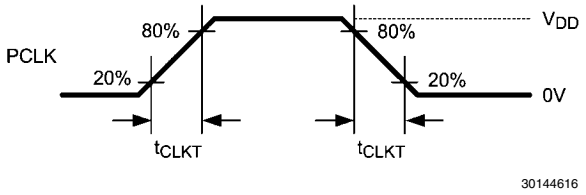


FIGURE 9. Serializer Input Clock Transition Times

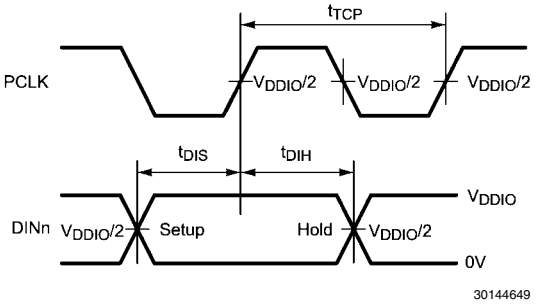


FIGURE 10. Serializer Setup/Hold Times

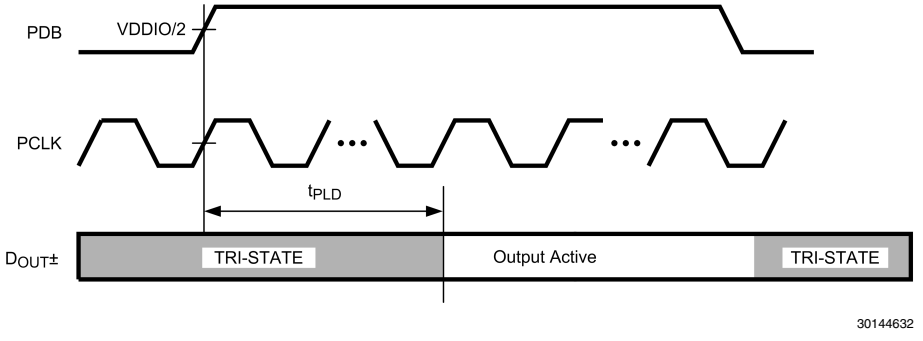


FIGURE 11. Serializer PLL Lock Time

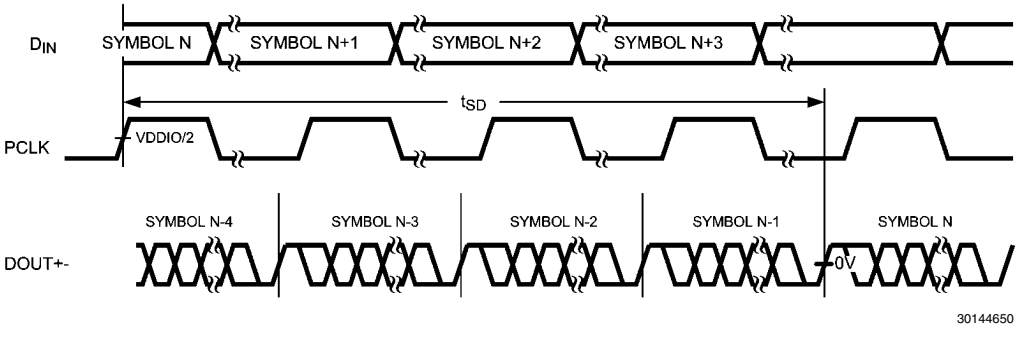


FIGURE 12. Serializer Delay

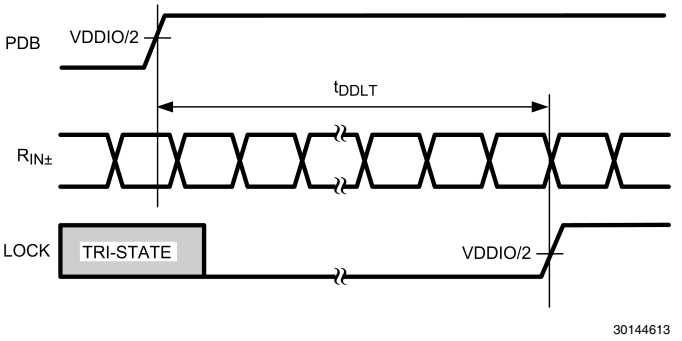


FIGURE 13. Deserializer Data Lock Time

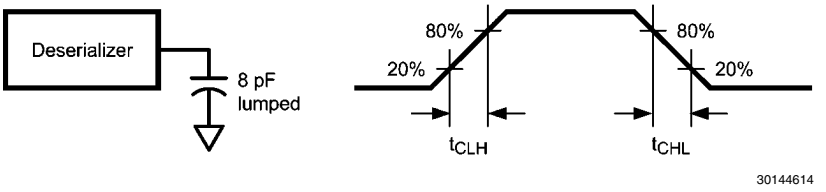


FIGURE 14. Deserializer LVCMOS Output Load and Transition Times

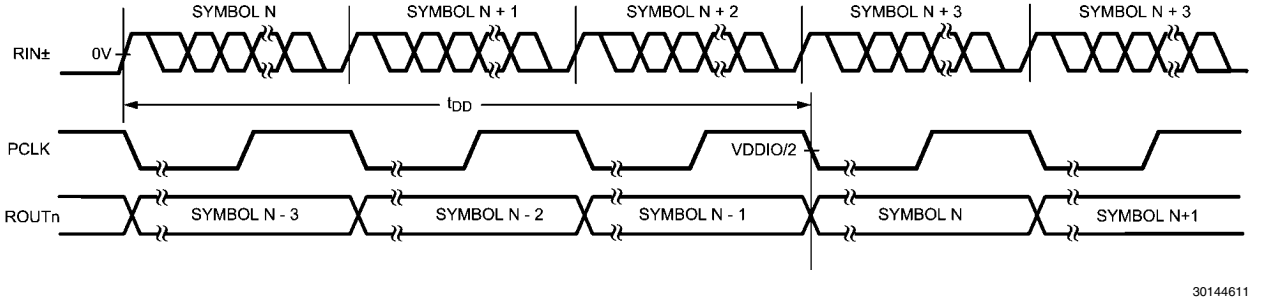


FIGURE 15. Deserializer Delay

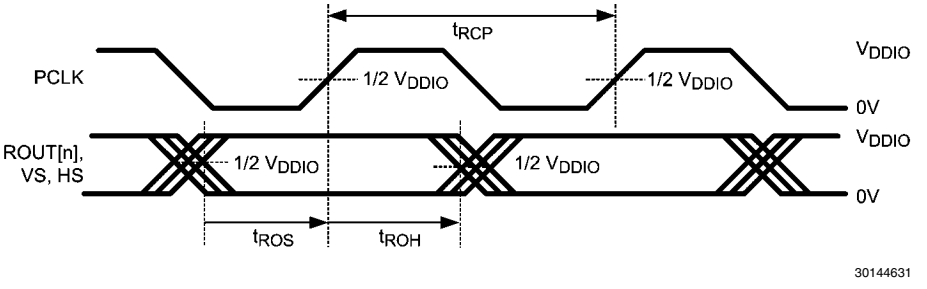


FIGURE 16. Deserializer Output Setup/Hold Times

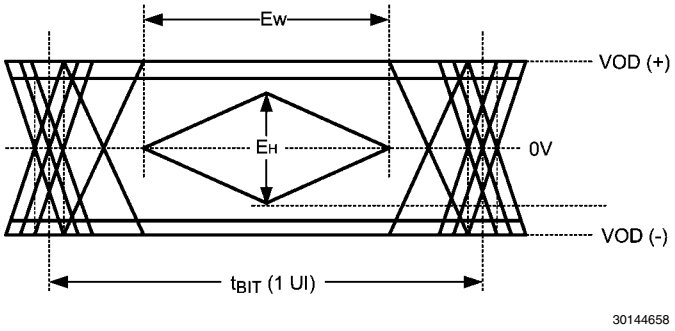


FIGURE 17. CML Output Driver

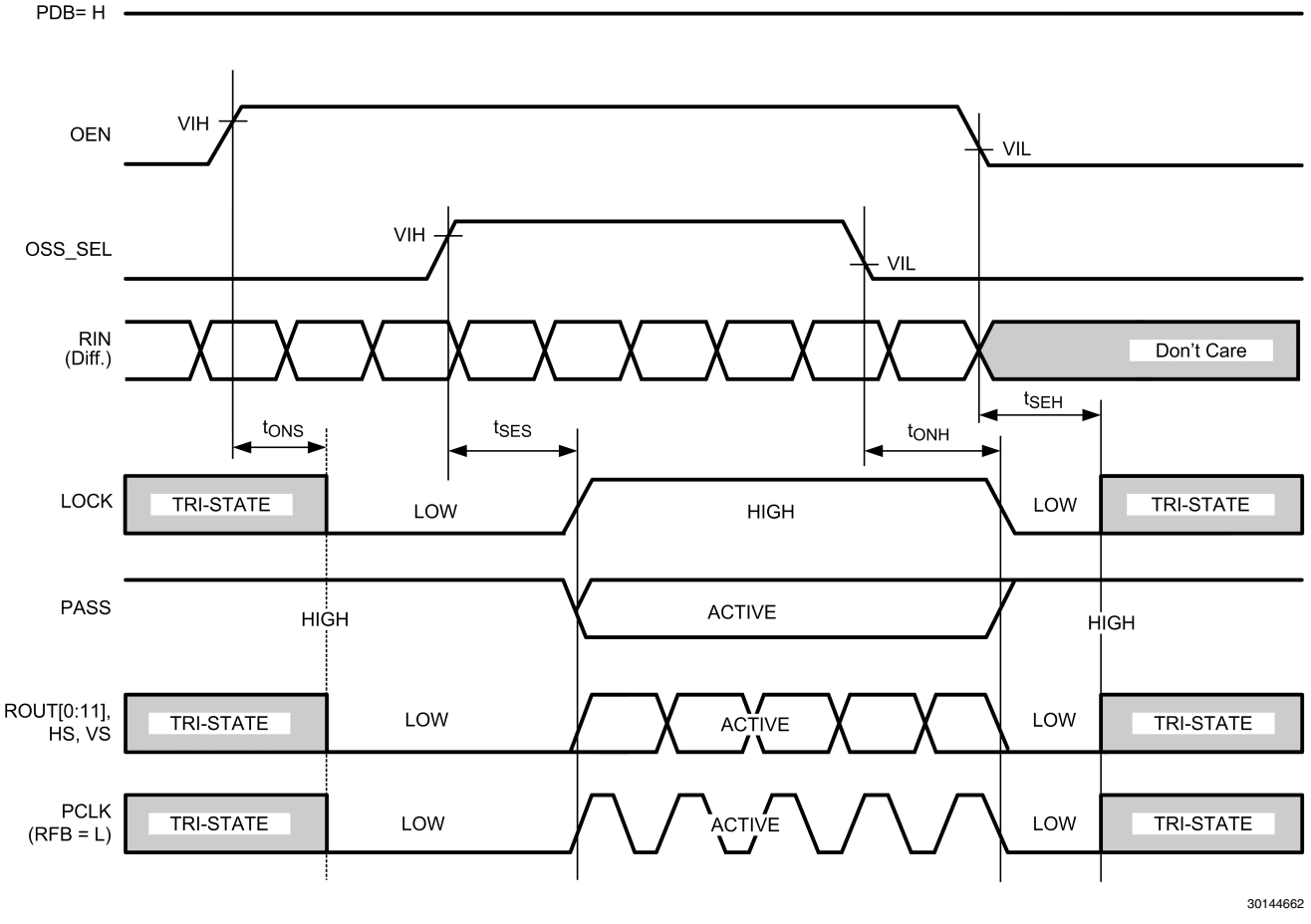


FIGURE 18. Output State (Setup and Hold) Times

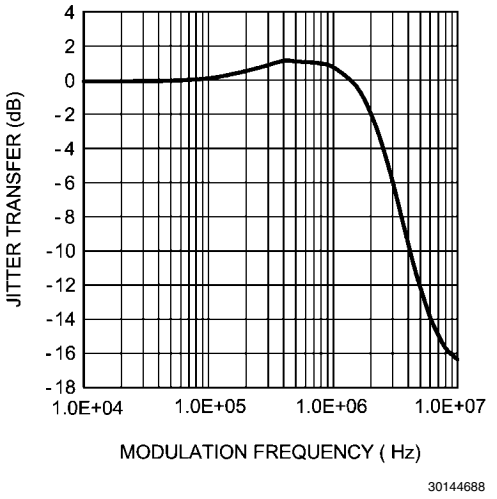


FIGURE 19. Typical Serializer Jitter Transfer Function at 100MHz

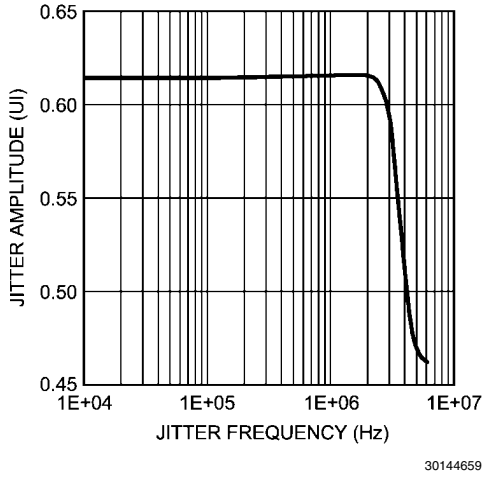


FIGURE 20. Typical Deserializer Input Jitter Tolerance Curve at 1.4Gbps Line Rate

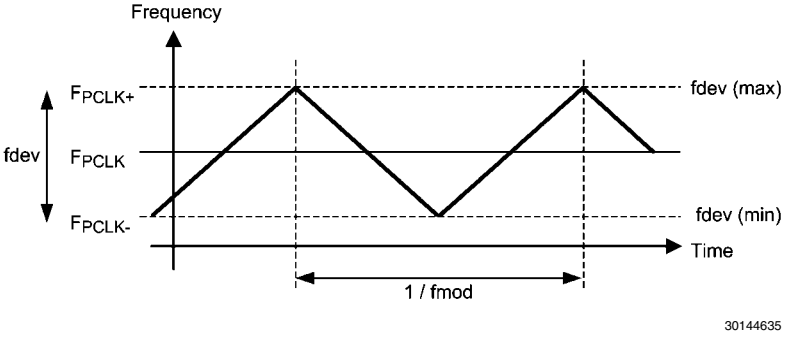


FIGURE 21. Spread Spectrum Clock Output Profile

TABLE 1. DS90UB913Q Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x00	I²C Device ID	7:1	DEVICE ID	RW	0x58'h	7-bit address of Serializer; 0x58'h (0101_1000X'b) default
		0	SER ID SEL			0: Device ID is from ID[x] 1: Register I²C Device ID overrides ID[x]
0x01	Power and Reset	7	RSVD			Reserved
		6	RDS	RW	0	Digital Output Drive Strength 1: High Drive Strength 0: Low Drive Strength
		5	VDDIO Control	RW	1	Auto Voltage Control 1: Enable 0: Disable
		4	VDDIO MODE	RW	1	V_{DDIO}Voltage set 0: 1.8V 1: 3.3V
		3	ANAPWDN	RW	0	This register can be set only through local I²C access 1: Analog power-down : Powers Down the analog block in the Serializer 0: No effect
		2	RSVD	RW	0	Reserved
		1	DIGITAL RESET1	RW	0	1: Resets the digital block except for register values values. Does not affect device I²C Bus or Device ID. This bit is self-clearing. 0: Normal Operation
		0	DIGITAL RESET0	RW	1	1: Digital Reset, resets the entire digital block including all register values.This bit is self-clearing. 0: Normal Operation.
0x02	**RESERVED**					

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x03	General Configuration	7	RX CRC Checker Enable	RW	1	Back-channel CRC Checker Enable 1:Enabled 0:Disabled
		6	TX Parity Generator Enable	RW	1	Forward channel Parity Generator Enable 1: Enable 0: Disable
		5	CRC Error Reset	RW	0	Clear CRC Error Counters. This bit is NOT self-clearing. 1: Clear Counters 0: Normal Operation
		4	I²C Remote Write Auto Acknowledge	RW	0	Automatically Acknowledge I2C Remote Write The mode works when the system is LOCKed. 1: Enable: When enabled, I²C writes to the Deserializer (or any remote I2C Slave, if I²C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. 0: Disable
		3	I²C Pass All	RW	0	1: Enable Forward Control Channel pass-through of all I²C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID. **The I²C accesses are then remapped to address specified in register 0x06.** 0: Enable Forward Control Channel pass-through only of I²C accesses to I²C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID.
		2	I²C PASSTHROUGH	RW	1	I²C Pass-Through Mode 0: Pass-Through Disabled 1: Pass-Through Enabled
		1	OV_CLK2PLL	RW	0	1:Enabled : When enabled this registers overrides the clock to PLL mode (External Oscillator mode or Direct PCLK mode) defined through MODE pin and allows selection through register 0x35 in the Serializer 0: Disabled : When disabled,cClock to PLL mode (External Oscillator mode or Direct PCLK mode) is defined through MODE pin on the Serializer.
		0	TRFB	RW	1	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
0x04	**RESERVED**					

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x05	Mode Select	7	RSVD	RW	0	Reserved
		6	RSVD	RW	0	Reserved.
		5	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from back-channel 1: Overrides MODE select bits 0: Does not override MODE select bits
		4	MODE_UP To DATE	R	0	Indicates that the status of mode select from Deserializer is up to date
		3	Pin_MODE_12–bit High Frequency	R	0	1: 12 bit high frequency mode is selected. 0: 12 bit high frequency mode is not selected.
		2	Pin_MODE_10–bit mode	R	0	1: 10 bit mode is selected. 0: 10 bit mode is not selected.
		1:0	RSVD			Reserved
0x06	DES ID	7:1	Desializer Device ID	RW	0x00	7-bit Deserializer Device ID Configures the I²C Slave ID of the remote Deserializer. A value of 0 in this field disables I²C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
		0	Freeze Device ID	RW	0	1: Prevents auto-loading of the Deserializer Device ID by the bidirectional control channel. The ID will be frozen at the value written. 0: Update
0x07	DESAlias	7:1	Deserializer ALIAS ID	RW	0	7-bit Remote Deserializer Device Alias ID Configures the decoder for detecting transactions designated for an I²C Deserializer device. The transaction will be remapped to the address specified in the DES ID register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x08	SlaveID	7:1	SLAVE ID	RW	0x00	7-bit Remote Slave Device ID Configures the physical I²C address of the remote I²C Slave device attached to the remote Deserializer. If an I²C transaction is addressed to the Slave Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote I²C slave.
		0	RSVD			Reserved
0x09	SlaveAlias	7:1	SLAVE ALIAS ID	RW	0x00	7-bit Remote Slave Device Alias ID Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0	Number of back-channel CRC errors during normal operation Least Significant byte

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0	Number of back-channel CRC errors during normal operation Most Significant byte
0x0C	General Status	7:5	Rev-ID	R	0	Revision ID 0x00: Production
		4	RX Lock Detect	R	0	1: RX LOCKED 0: RX not LOCKED
		3	BIST CRC Error Status	R	0	1: CRC errors in BIST mode 0: No CRC errors in BIST mode
		2	PCLK Detect	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
		1	DES Error	R	0	1: CRC error is detected during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04. 0: No effect
		0	LINK Detect	R	0	1: Cable link detected 0: Cable link not detected This includes any of the following faults — Cable Open — '+' and '-' shorted — Short to GND — Short to battery
0x0D	GPO[0] and GPO[1] Configuration	7	GPO1 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO1 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO1 Direction	RW	0	1: Input 0: Output
		4	GPO0 Enable	RW	1	1: GPIO enable 0: Tri-state
		3	GPO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO0 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	GPO0 Direction	RW	0	1: Input 0: Output
		0	GPO0 Enable	RW	1	1: GPIO enable 0: Tri-state

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x0E	GPO[2] and GPO[3] Configuration	7	GPO3 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO3 Remote Enable	RW	0	Remote GPIO Control 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		5	GPO3 Direction	RW	1	1: Input 0: Output
		4	GPO3 Enable	RW	1	1: GPIO enable 0: Tri-state
		3	GPO2 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO2 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote Deserializer. The GPIO pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
		1	GPO2 Direction	RW	0	1: Input 0: Output
		0	GPO2 Enable	RW	1	1: GPIO enable 0: Tri-state

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x0F	I²C Master Config	7:5	RSVD			Reserved
		4:3	SDA Output Delay	RW	00	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : 350ns 01: 400ns 10: 450ns 11: 500ns
		2	Local Write Disable	RW	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I²C master attached to the Deserializer. Setting this bit does not affect remote access to I²C slaves at the Serializer.
		1	I2C Bus Timer Speed up	RW	0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
		0	I2C Bus Timer Disable	RW	0	1. Disable I²C Bus Watchdog Timer When the I²C Watchdog Timer may be used to detect when the I²C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I²C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL 0: No effect
0x10	I2C Control	7	RSVD			Reserved
		6:4	SDA Hold Time	RW	0x1	Internal SDA Hold Time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I2C Filter Depth	RW	0x7	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10ns.
0x11	SCL High Time	7:0	SCL High Time	RW	0x82	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4µs + 1µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x12	SCL LOW Time	7:0	SCL Low Time	RW	0x82	I²C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I²C bus. This value is also used as the SDA setup time by the I²C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7µs + 0.3µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x13	General Purpose Control	7:0	GPCR[7:0]	RW	0	1: High 0: Low
0x14	BIST Control	7:3	RSVD			Reserved
		2:1	Clock Source	RW	0x0	Allows choosing different OSC clock frequencies for forward channel frame. OSC Clock Frequency in Functional Mode when OSC mode is selected or when the selected clock source is not present e.g. missing PCLK/ External Oscillator. See *Table 3* for oscillator clock frequencies when PCLK/ External Clock is missing.
		0	BIST Enable	RW	0	BIST Control: 1: Enable BIST mode 0: Disable BIST mode
0x15–0x1D	**RESERVED**					
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	RW	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
0x1F-0x29	**RESERVED**					
0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0	Number of CRC Errors in the back channel when in BIST mode
0x2B-0x34	**RESERVED**					
0x35	PLL Clock Overwrite	7:4	RSVD			Reserved
		3	PIN_LOCK to External Oscillator	RW	0	Status of mode select pin 1: Indicates External Oscillator mode is selected by mode-resistor 0: External Oscillator mode is not selected by mode-resistor
		2	PIN_LOCK2Oscillator	RW	0	Status of mode select pin 1: Indicates PCLK mode is selected by mode-resistor 0: PCLK mode not selected by mode-resistor
		1	LOCK to External Oscillator	RW	0	Affects only when 0x03[1]=1 (OV_CLK2PLL) and 0x35 [0]=0. 1: Routes GPO3 directly to PLL 0: Allows PLL to lock to PCLK"
		0	RSVD			Reserved

TABLE 2. DS90UB914Q Control Registers

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x00	I²C Device ID	7:1	DEVICE ID	RW	0x60'h	7-bit address of Deserializer; 0x60h
		0	Deserializer ID Select	RW	0	0: De-Serializer Device ID is set using address coming from CAD 1: Register I²C Device ID overrides ID[x]
0x01	Reset	7:6	RSVD			Reserved
		5	ANAPWDN	RW	0	This register can be set only through local I²C access 1: Analog power-down : Powers Down the analog block in the Serializer 0: No effect
		4:2	RSVD			Reserved
		1	Digital Reset 1	RW	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: No effect
		0	Digital Reset 0	RW	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: No effect
0x02	General Configuration 0	7	RSVD			Reserved
		6	RSVD			Reserved
		5	Auto-Clock	RW	0	1: Output PCLK or OSC clock when not LOCKED 0: Only PCLK
		4	SSCG LFMODE	RW	0	1: Selects 8x mode for 10-18 MHz frequency range in SSCG 0: SSCG running at 4X mode
		3:0	SSCG	RW	0	SSCG Select 0000: Normal Operation, SSCG OFF 0001: fmod (kHz) PCLK/2168, fdev +/-0.50% 0010: fmod (kHz) PCLK/2168, fdev +/-1.00% 0011: fmod (kHz) PCLK/2168, fdev +/-1.50% 0100: fmod (kHz) PCLK/2168, fdev +/-2.00% 0101: fmod (kHz) PCLK/1300, fdev +/-0.50% 0110: fmod (kHz) PCLK/1300, fdev +/-1.00% 0111: fmod (kHz) PCLK/1300, fdev +/-1.50% 1000: fmod (kHz) PCLK/1300, fdev +/-2.00% 1001: fmod (kHz) PCLK/868, fdev +/-0.50% 1010: fmod (kHz) PCLK/868, fdev +/-1.00% 1011: fmod (kHz) PCLK/868, fdev +/-1.50% 1100: fmod (kHz) PCLK/868, fdev +/-2.00% 1101: fmod (kHz) PCLK/650, fdev +/-0.50% 1110: fmod (kHz) PCLK/650, fdev +/-1.00% 1111: fmod (kHz) PCLK/650, fdev +/-1.50% Note: **This regsiter should be changed only after disabling SSCG.**

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x03	General Configuration 1	7	RX Parity Checker Enable	RW	1	Forward Channel Parity Checker Enable 1: Enable 0: Disable
		6	TX CRC Checker Enable	RW	1	Back Channel CRC Generator Enable 1: Enable 0: Disable
		5	V_{DDIO} Control	RW	1	Auto voltage control 1: Enable (auto detect mode) 0: Disable
		4	V_{DDIO} Mode	RW	0	VDDIO voltage set 1: 3.3V 0: 1.8V
		3	I²C Passthrough	RW	1	I²C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
		2	AUTO ACK	RW	0	Automatically Acknowledge I²C Remote Write When enabled, I²C writes to the Deserializer (or any remote I²C Slave, if I²C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. This allows I2C bus without LOCK. 1: Enable 0: Disable
		1	Parity Error Reset	RW	0	Parity Error Reset, This bit is self-clearing. 1: Parity Error Reset 0: No effect
		0	RRFB	RW	1	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Falling Clock Edge. 0: Parallel Interface Data is strobed on the Rising Clock Edge.
0x04	EQ Feature Control 1	7:0	EQ level - when AEQ bypass is enabled EQ setting is provided by this register	RW	0x00	Equalization gain 0x00 = ~0.0 dB 0x01 = ~4.5 dB 0x03 = ~6.5 dB 0x07 = ~7.5 dB 0x0F = ~8.0 dB 0x1F = ~11.0 dB 0x3F = ~12.5 dB
0x05	**RESERVED**					
0x06	SER ID	7:1	Remote ID	RW	0x0C	Remote Serializer ID
		0	Freeze Device ID	RW	0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x07	SER Alias	7:1	Serializer Alias ID	RW	0x00	7-bit Remote Serializer Device Alias ID Configures the decoder for detecting transactions designated for an I²C Deserializer device. The transaction will be remapped to the address specified in the SER ID register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x08	Slave ID[0]	7:1	Slave ID0	RW	0	7-bit Remote Slave Device ID 0 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x09	Slave ID[1]	7:1	Slave ID1	RW	0	7-bit Remote Slave Device ID 1 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x0A	Slave ID[2]	7:1	Slave ID2	RW	0x00	7-bit Remote Slave Device ID 2 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x0B	Slave ID[3]	7:1	Slave ID3	RW	0	7-bit Remote Slave Device ID 3 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x0C	Slave ID[4]	7:1	Slave ID4	RW	0	7-bit Remote Slave Device ID 4 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x0D	Slave ID[5]	7:1	Slave ID5	RW	0x00	7-bit Remote Slave Device ID 5 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID5 , the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x0E	Slave ID[6]	7:1	Slave ID6	RW	0	7-bit Remote Slave Device ID 6 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x0F	Slave ID[7]	7:1	Slave ID7	RW	0x00	7-bit Remote Slave Device ID 7 Configures the physical I²C address of the remote I²C Slave device attached to the remote Serializer. If an I²C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
		0	RSVD			Reserved
0x10	Slave Alias[0]	7:1	Slave Alias ID0	RW	0x00	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x11	Slave Alias[1]	7:1	Slave Alias ID1	RW	0x00	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x12	Slave Alias[2]	7:1	Slave Alias ID2	RW	0x00	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x13	Slave Alias[3]	7:1	Slave Alias ID3	RW	0x00	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x14	Slave Alias[4]	7:1	Slave Alias ID4	RW	0x00	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x15	Slave Alias[5]	7:1	Slave Alias ID5	RW	0x00	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x16	Slave Alias[6]	7:1	Slave Alias ID6	RW	0x00	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x17	Slave Alias[7]	7:1	Slave Alias ID7	RW	0x00	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I²C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I²C Slave.
		0	RSVD			Reserved
0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	RW	0	Parity errors threshold on the Forward channel during normal information. This sets the maximum number of parity errors that can be counted using register 0x1A. Least significant Byte.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	RW	0	Parity errors threshold on the Forward channel during normal operation. This sets the maximum number of parity errors that can be counted using register 0x1B. Most significant Byte
0x1A	Parity Errors	7:0	Parity Error Byte 0	RW	0	Number of parity errors in the Forward channel during normal operation. Least significant Byte
0x1B	Parity Errors	7:0	Parity Error Byte 1	RW	0	Number of parity errors in the Forward channel during normal operation Most significant Byte
0x1C	General Status	7:4	Rev-ID	R	0	Revision ID 0x0000: Production
		3	RSVD			Reserved
		2	Parity Error	R	0	Parity Error detected 1: Parity Errors detected 0: No Parity Errors
		1	Signal Detect	R	0	1: Serial input detected 0: Serial input not detected
		0	Lock	R	0	De-Serializer CDR, PLL's clock to recovered clock frequency 1: De-Serializer locked to recovered clock 0: De-Serializer not locked
0x1D	GPIO[1] and GPIO[0] Config	7	GPIO1 Output Vaue	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved
		5	GPIO1 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		4	GPIO1 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
		3	GPIO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved
		1	GPIO0 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		0	GPIO0 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x1E	GPIO[3] and GPIO[2] Config	7	GPIO3 Output Vaue	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved
		5	GPIO3 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		4	GPIO3 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
		3	GPIO2 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved
		1	GPIO2 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		0	GPIO2 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
0x1F	Mode and OSS Select	7	OEN_OSS Override	RW	0	Allows overriding OEN and OSS select coming from Pins 1: Overrides OEN/OSS_SEL selected by pins 0: Does NOT override OEN/OSS_SEL select by pins
		6	OEN Select	RW	0	OEN configuration from register
		5	OSS Select	R	0	OSS_SEL configuration from register
		4	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from back-channel 1: Overrides MODE select bits 0: Does not override MODE select bits
		3	PIN_MODE_12–bit HF mode	R	0	Status of mode select pin
		2	PIN_MODE_10 bit mode	R	0	Status of mode select pin
		1	MODE_12–bit High Frequency	RW	0	Selects 12 bit high frequency mode. This bit is automatically updated by the mode settings from RX unless MODE_OVERRIDE is SET 1: 12 bit high frequency mode is selected. 0: 12 bit high frequency mode is not selected.
		0	MODE_10–bit mode	RW	0	Selects 10 bit mode. This bit is automatically updated by the mode settings from RX unless MODE_OVERRIDE is SET 1: Enables 10 bit mode. 0: Disables 10 bit mode.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x20	BCC Watchdog Control	7:1	BCC Watchdog timer	RW	0	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
0x21	I²C Control 1	7	I²C pass through all	RW	0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
		6:4	I²C SDA Hold	RW	0	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I²C Filter Depth	RW	0	I²C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10ns.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x22	I²C Control 2	7	Forward Channel Sequence Error	R	0	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. 1: If this bit is set, an error may have occurred in the control channel operation 0: No forward channel errors have been detected on the control channel
		6	Clear Sequence Error	RW	0	Clears the Sequence Error Detect bit
		5	RSVD			Reserved
		4:3	SDA Output Delay	RW	0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : 350ns 01: 400ns 10: 450ns 11: 500ns
		2	Local Write Disable	RW	0	Disable Remote Writes to local registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
		1	I²C Bus Timer Speedup	RW	0	Speed up I²C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50µs 0: Watchdog Timer expires after approximately 1s.
		0	I²C Bus Timer Disable	RW	0	Disable I²C Bus Watchdog Timer When the I²C Watchdog Timer may be used to detect when the I²C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I²C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
0x23	General Purpose Control	7:0	GPCR	RW	0	Scratch Register
0x24	BIST Control	7:4	RSVD			Reserved
		3	BIST Pin Configuration	RW	1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through register bit "reg_24 [0]"
		2:1	BIST Clock Source	RW	00	BIST Clock Source See *Table 4*
		0	BIST Enable	RW	0	BIST Control 1: Enabled 0: Disabled
0x25	Parity Error Count	7:0	BIST Error Count	R	0	Number of Forward channel Parity errors in the BIST mode.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
0x26–0x3B	**RESERVED**					
0x3C	Oscillator output divider select	7:2	RSVD			Reserved
		1:0	OSC OUT DIVIDER SEL	RW	0	Selects the divider for the OSC clock out on PCLK when system is not locked and selected by OEN/OSSSEL 0x02[5] 00: 50M (+/- 30%) 01: 25M (+/- 30%) 1X: 12.5M (+/- 30%)
0x3D-0x3E	**RESERVED**					
0x3F	CML Output Enable	7:5	RSVD			Reserved
		4	CML OUT Enable	RW	1	0: CML Loop-through Driver is powered up 1: CML Loop-through Driver is powered down.
		3:0	RSVD			Reserved
0x40	SCL High Time	7:0	SCL High Time	RW	0x82	I²C Master SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Master on the local I²C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4µs + 0.3µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x41	SCL Low Time	7:0	SCL Low Time	RW	0x82	I²C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I²C bus. This value is also used as the SDA setup time by the I²C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7µs + 0.3µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x42	CRC Force Error	7:2	RSVD			Reserved
		1	Force Back Channel Error	RW	0	1: This bit introduces multiple errors into Back channel frame. 0: No effect
		0	Force One Back Channel Error	RW	0	1: This bit introduces ONLY one error into Back channel frame. Self clearing bit 0: No effect
0x43-0x4C	**RESERVED**					
0x4D	AEQ Test Mode Select	7	RSVD			Reserved
		6	AEQ Bypass	RW	0	Bypass AEQ and use set manual EQ value using register 0x04
		5:0	RSVD			Reserved
0x4E	EQ Value	7:0	AEQ / Manual Eq Readback	R	0	Read back the adaptive and manual Equalization value

TABLE 3. Clock Sources for Forward Channel Frame on the Serializer During Normal Operation

DS90UB913Q Reg 0x14 [2:1]	10–bit Mode	12–bit High Frequency Mode	12–bit Low Frequency Mode
00	50 MHz	37.5 MHz	25 MHz
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	25MHz	18.75 MHz	12.5 MHz

TABLE 4. BIST Clock Sources

DS90UB914Q Reg 0x24 [2:1]	10–bit Mode	12–bit High Frequency Mode	12–bit Low Frequency Mode
00	PCLK	PCLK	PCLK
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	25MHz	18.75 MHz	12.5 MHz

Functional Description

The DS90UB913/914Q FPD- Link III chipsets are intended to link mega-pixel camera imagers and video processors in ECUs. The Serializer/Deserializer chipset can operate from 10MHz to 100MHz pixel clock frequency. The DS90UB913Q device transforms a 10/12-bit wide parallel LVCMOS data bus along with a bidirectional control channel control bus into a single high-speed differential pair. The high speed serial bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB914Q device receives the single serial data stream and converts it back into a 10/12-bit wide parallel data bus together with the control channel data bus. The DS90UB913/914Q chipsets can accept up to

- 12 bits of DATA+2 bits SYNC for an input PCLK range of 10MHz-50MHz in the 12-bit low frequency mode
- 12 bits DATA + 2 SYNC bits for an input PCLK range of 15MHz to 75MHz in the 12-bit high frequency mode
- 10 bits DATA + 2 SYNC bits for an input PCLK range of 20MHz to 100MHz in the 10-bit mode.

The DS90UB914Q chipset has a 2:1 multiplexer which allows customers to select between two Serializer inputs. The control channel function of the DS90UB913/DS90UB914Q chipset provides bidirectional communication between the image sensor and ECUs. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bidirectional control channel bus is controlled via an I2C port. The bidirectional control channel offers asymmetrical communication and is not dependent on video blanking intervals.

The DS90UB913/914Q chipset offer customers the choice to work with different clocking schemes. The DS90UB913/914Q chipsets can use an external oscillator as the reference clock source for the PLL or PCLK from the imager as primary reference clock to the PLL.

Transmission Media

The DS90UB913/914Q chipset is intended to be used in a point-to-point configuration through a shielded twisted pair cable. The Serializer and Deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100 Ohms. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board(discontinuities, power plane), the electrical environment (e.g power stability, ground noise, input clock jitter, PCLK frequency, etc). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. A differential probe should be used to measure across the termination resistor at the CMLOUTP/N pins. *Figure 17* illustrates the minimum eye width and eye height that is necessary for bit error free operation.

DS90UB913/914Q Operation with External Oscillator as Reference Clock

In some applications, the pixel clock that comes from the imager can have jitter which exceeds the tolerance of the DS90UB913/914Q chipsets. In this case, the DS90UB913Q device should be operated by using an external clock source as the reference clock for the DS90UB913/914Q chipsets. **This is the recommended operating mode.** The external oscillator clock output goes through a divide-by-2 circuit in the DS90UB913Q Serializer and this divided clock output is used as the reference clock for the imager. The output data and pixel clock from the imager are then fed into the DS90UB913Q device. *Figure 22* shows the operation of the DS90UB13/914Q chipsets while using an external automotive grade oscillator.

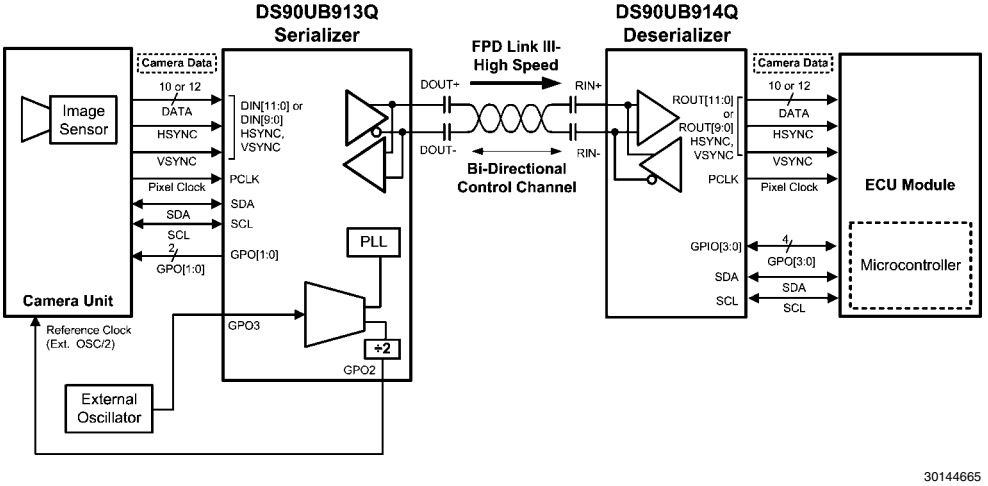


FIGURE 22. DS90UB913/914Q Operation in the External Oscillator Mode

When the DS90UB913Q device is operated using an external oscillator, the GPO3 pin on the DS90UB913Q is the input pin for the external oscillator. In applications where the DS90UB913Q device is operated from an external oscillator, the divide-by-2 circuit in the DS90UB913Q device feeds back the divided clock output to the imager device through GPO2 pin. The pixel clock to external oscillator ratios needs to be fixed for the 12–bit high frequency mode and the 10–bit mode. **In the 10-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 2. In the 12-bit high frequency mode, the pixel clock frequency divided by the external oscillator frequency must be 1.5.** For example, if the external oscillator frequency is 48MHz in the 10–bit mode, the pixel clock frequency of the imager needs to be twice of the external oscillator frequency, i.e. 96MHz. If the external oscillator frequency is 48MHz in the 12-bit high frequency mode, the pixel clock frequency of the imager needs to be 1.5 times of the external oscillator frequency, i.e. 72MHz. In this mode, GPO2 and GPO3 on the Serializer cannot act as the output of the input signal coming from GPIO2 or GPIO3 on the Deserializer.

DS90UB913/914Q Operation with Pixel Clock from Imager as Reference Clock

The DS90UB913/914Q chipsets can be operated by using the pixel clock from the imager as the reference clock. *Figure 23* shows the operation of the DS90UB913/914Q chipsets using the pixel clock from the imager. If the DS90UB913Q device is operated using the pixel clock from the imager as the reference clock, then the imager uses an external oscillator as its reference clock. There are 4 GPIOs on the Serializer and 4 GPIOs on the Deserializer in this mode.

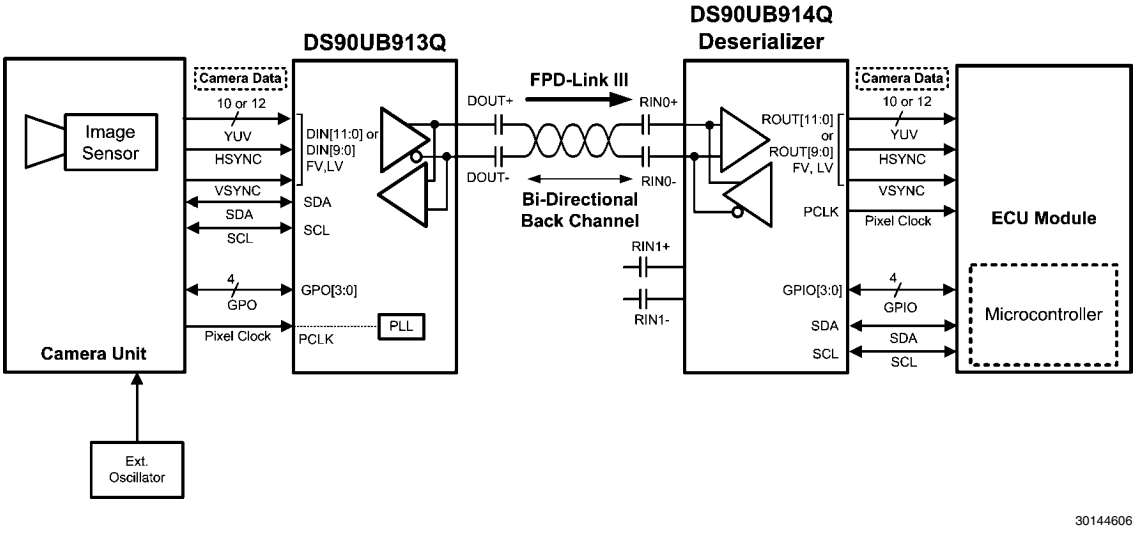


FIGURE 23. DS90UB913Q/914Q Operation in PCLK mode

MODE Pin on Serializer

The mode pin on the Serializer can be configured to select if the DS90UB913Q device is to be operated from the external oscillator or the PCLK from the imager. The pin must be pulled to V_{DD}(1.8V, not V_{DDIO}) with a 10 kΩ resistor and a pull down resistor (R_{MODE}) of the recommended value to set the modes shown in *Figure 24*. The recommended maximum resistor tolerance is 1%.

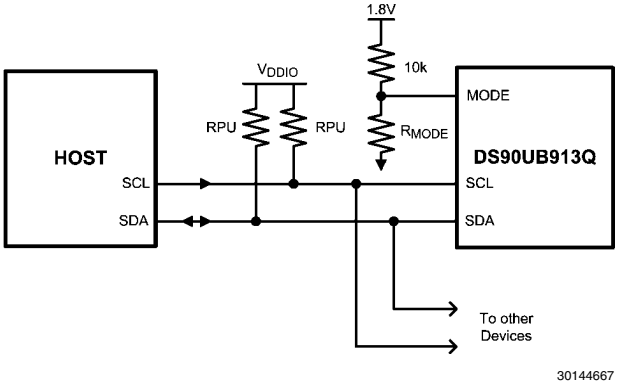


FIGURE 24. MODE Pin configuration on DS90UB913Q

TABLE 5. DS90UB913Q Serializer MODE Resistor Value

DS90UB913Q Serializer MODE Resistor Value	
Mode Select	**R_{MODE} Resistor Value**
PCLK from imager mode	0kΩ
External Oscillator mode	4.7kΩ

MODE Pin on Deserializer

The mode pin on the Deserializer can be used to configure the device to work in the 12-bit low frequency mode, 12- bit high frequency mode or the 10 bit mode of operation. Internally, the DS90UB913/914Q chipset operates in a divide-by-1 mode in the 12- bit low frequency mode, divide-by-2 mode in the 10-bit mode and a divide-by-1.5 mode in the 12- bit high frequency mode. The pin must be pulled to V_{DD}(1.8V, not V_{DDIO}) with a 10 kΩ resistor and a pull down resistor (R_{MODE}) of the recommended value to set the different modes in the Deserializer as mentioned in . The Deserializer automatically configures the Serializer to correct mode via the back-channel. The recommended maximum resistor tolerance is 1%

.

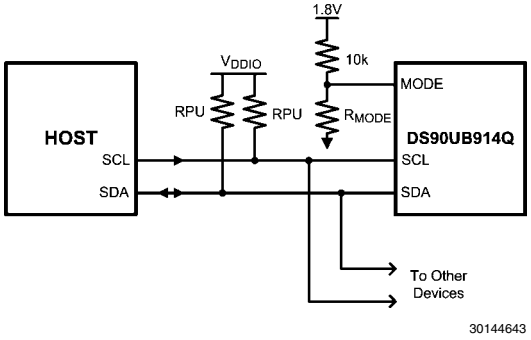


FIGURE 25. Mode Pin Configuration on DS90UB914Q Deserializer

TABLE 6. DS90UB914Q Deserializer MODE Resistor Value

DS90UB914Q Deserializer MODE resistor Value	
MODE Select	**R_{MODE} Resistor Value**
12-bit low frequency mode 10-50 MHz PCLK, 10/12 bits DATA+ 2 SYNC	0kΩ
12-bit high frequency mode 15-75 MHz PCLK, 10/12 bits DATA+ 2 SYNC	3kΩ
10-bit mode 20 MHz – 100 MHz PCLK, 10 bits DATA+ 2 SYNC	11kΩ

Line Rate Calculations for the DS90UB913/914Q

The DS90UB913Q device divides the clock internally by divide-by-1 in the 12 bit low frequency mode, by divide-by-2 in the 10-bit mode and by divide-by-1.5 in the 12-bit high frequency mode. Conversely, the DS90UB914Q multiplies the recovered serial clock to generate the proper pixel clock output frequency. Thus the maximum line rate in the three different modes remains 1.4Gbps. The following are the formulae used to calculate the maximum line rate in the different modes.

- For 12 bit low frequency mode, Line rate = f_{PCLK}*28; e.g. f_{PCLK}=50MHz, line rate = 50*28=1.4Gbps
- For 10 bit mode, Line rate = f_{PCLK}/2*28; e.g. f_{PCLK}=100MHz, line rate = (100/2)*28=1.4Gbps
- For the 12 bit high frequency mode, Line rate = f_{PCLK}*(2/3)*28; e.g. f_{PCLK}=75MHz, line rate = (75)*(2/3)*28=1.4Gbps

Deserializer Multiplexer Input

The DS90UB914Q offers a 2:1 multiplexer that can be used to select which camera is used as the input. *Figure 26* shows the operation of the 2:1 multiplexer in the Deserializer. The selection of the camera can be pin controlled as well as register controlled. Both the Deserializer inputs cannot be enabled at the same time. If the Serializer A is selected as the active Serializer, the back-channel for Deserializer A turns ON and vice versa. To switch between the two cameras, first the Serializer B has to be selected

using the SEL pin/register on the Deserializer. After that the back channel driver for Deserializer B has to be enabled using the register in the Deserializer.

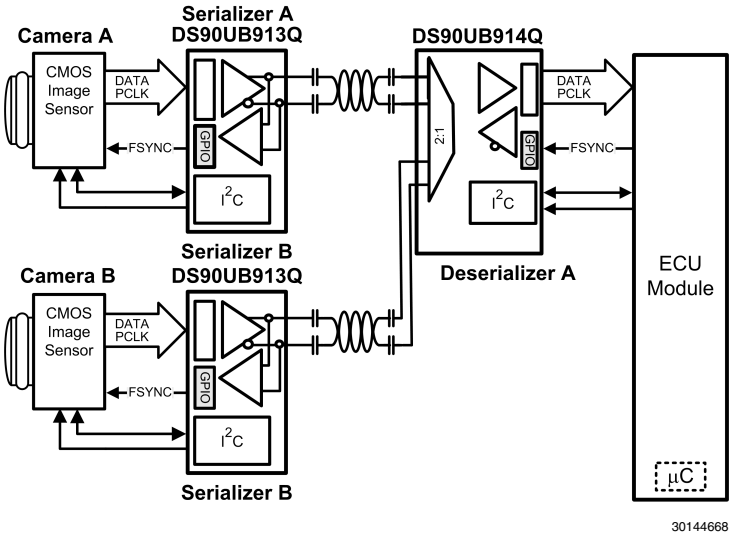


FIGURE 26. Using the multiplexer on the Deserializer to enable a two camera system

Serial Frame Format

The High Speed Forward Channel is composed of 28 bits of data containing video data, sync signals, I2C and parity bits. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled. The 28 bits frame structure changes in the 12 bit low frequency mode, 12 bit high frequency mode and the 10 bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low speed forward and backward path across the serial link together with a high speed forward channel without the dependence on the video blanking phase.

Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional control channel data across the serial link
- Parallel video/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 CRC bits on the back channel for error detection purposes. The DS90UB913/914Q chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the Serializer and the Deserializer respectively.

To check parity errors on the forward channel, monitor registers 0x1A and 0x1B on the Deserializer. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset.**Whenever there is a parity error on the forward channel, the PASS pin will go low.**

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the Serializer.

Description of Bidirectional Control Bus and I2C Modes

The I2C compatible interface allows programming of the DS90UB913Q, DS90UB914Q, or an external remote device (such as image sensor) through the bidirectional control channel. Register programming transactions to/from the DS90UB913Q/914Q chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to VDDIO by an external resistor. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UB913/914Q I2C bus data rate supports up to 400 kbps according to I2C fast mode specifications.

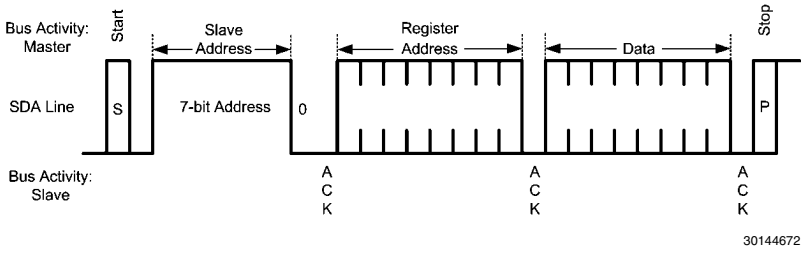


FIGURE 27. Write Byte

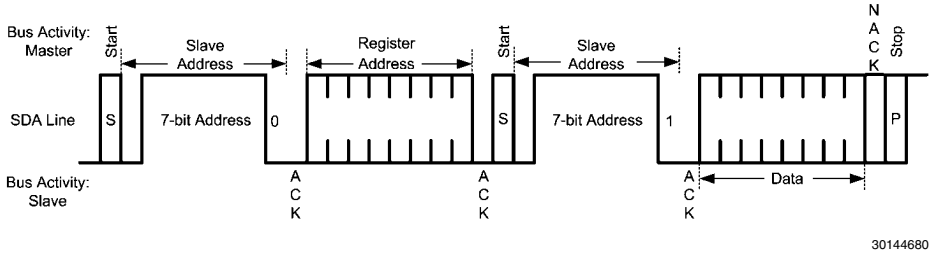


FIGURE 28. Read Byte

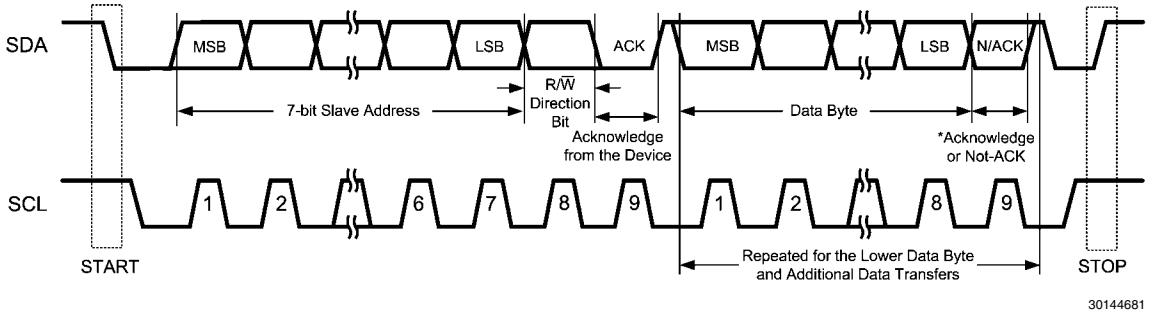


FIGURE 29. Basic Operation

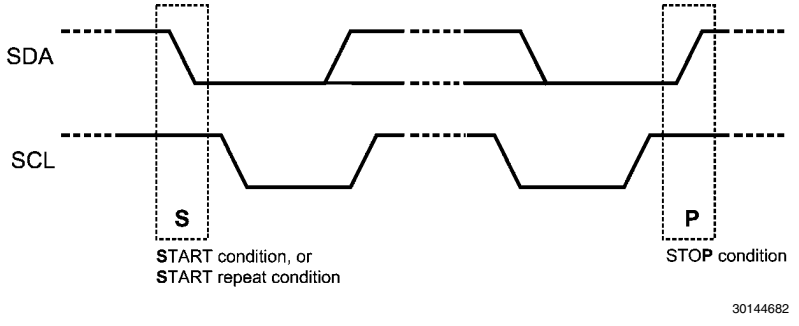


FIGURE 30. Start and Stop Conditions

Slave Clock Stretching

The I2C compatible interface allows programming of the DS90UB913Q, DS90UB914Q, or an external remote device (such as image sensor) through the bidirectional control To communicate and synchronize with remote devices on the I2C bus through the bidirectional control channel/MCU, **the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission**; where the I2C slave pulls the SCL line low on the 9th clock of every I2C transfer (before the ACK signal). The slave device

will not control the clock and only stretches it until the remote peripheral has responded. The I2C master must support clock stretching to operate with the DS90UB913/914Q chipset.

I2C Pass Through

I2C pass-through provides an alternative means to independently address slave devices. The mode enables or disables I2C bidirectional control channel communication to the remote I2C bus. This option is used to determine whether or not an I2C instruction is to be transferred over to the remote I2C device. When enabled, the I2C bus traffic will continue to pass through, I2C commands will be excluded to the remote I2C device. The pass through function also provides access and communication to only specific devices on the remote bus.

See *Figure 31* for an example of this function.

If master controller transmits I²C transaction for address 0xA0, the SER A with I²C pass through enabled will transfer I²C commands to remote Camera A. The SER B with I²C pass through disabled, any I²C commands will be bypassed on the I²C bus to Camera B.

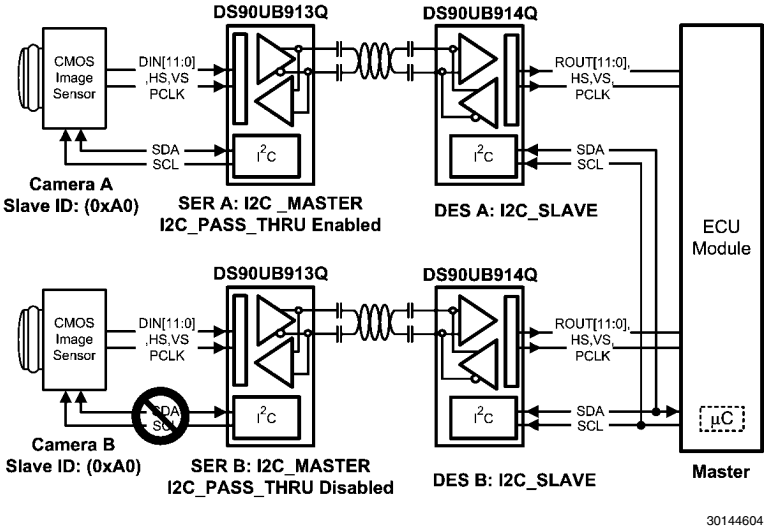


FIGURE 31. I²C Pass Through

ID[x] Address Decoder on the Serializer

The ID[x] pin on the Serializer is used to decode and set the physical slave address of the Serializer (I2C only) to allow up to five devices on the bus connected to the Serializer using only a single pin. The pin sets one of the 5 possible addresses for each Serializer device. The pin must be pulled to VDD (1.8V, not VDDIO) with a 10 kΩ resistor and a pull down resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

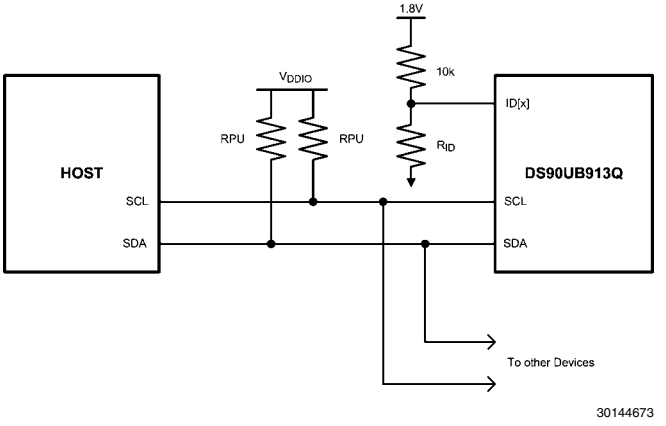


FIGURE 32. ID[x] Address Decoder on the Serializer

TABLE 7. ID[x] Resistor Value for DS90UB913Q Serializer

ID[x] Resistor Value — DS90UB913Q Serializer		
Resistor RID0 Ω (1% Tolerance)	**Address 7'b**	**Address 8'b 0 appended (WRITE)**
0k	0x58	0xB0
2k	0x59	0xB2
4.7k	0x5A	0xB4
8.2k	0x5B	0xB6
14k	0x5C	0xB8
100k	0x5D	0xBA

ID[x] Address Decoder on the Deserializer

The IDx[0] and IDx[1] pins on the Deserializer are used to decode and set the physical slave address of the Deserializer (I2C only) to allow up to 16 devices on the bus using only two pins. The pins set one of 16 possible addresses for each Deserializer device. As there will be more Deserializer devices connected on the same board than Serializers, more I2C device addresses have been defined for the DS90UB914Q Deserializer than the DSDS90UB913Q Serializer. The pins must be pulled to VDD (1.8V, not VDDIO) with a 10 kΩ resistor and two pull down resistors (RID0 and RID1) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

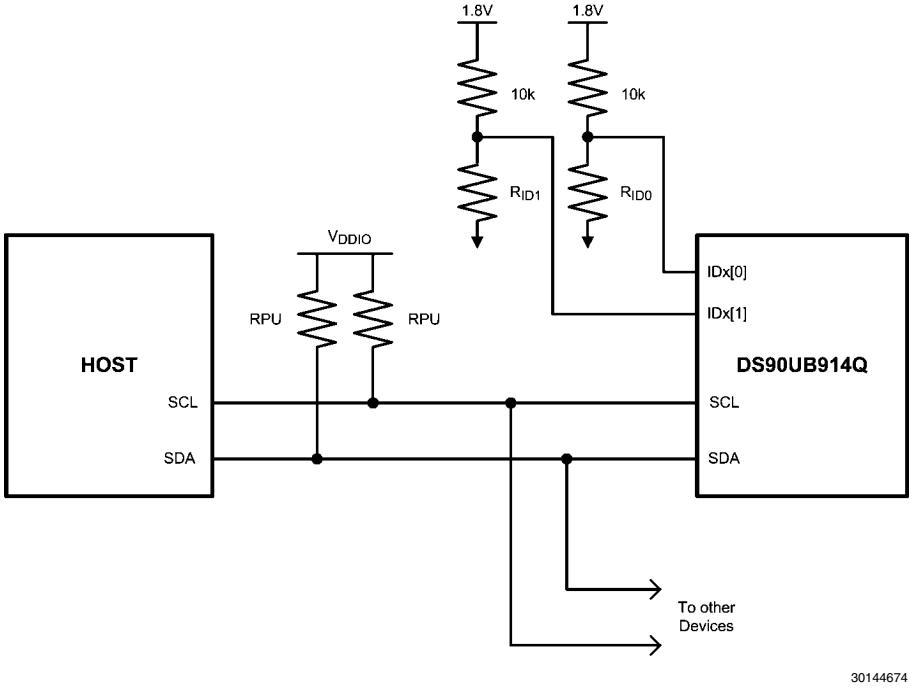


FIGURE 33. ID[x[Address Decoder on the Deserializer

TABLE 8. Resistor Values for IDx[0] and IDx[1] on DS90UB914Q Deserializer

ID[x] Resistor Value — DS90UB913Q Serializer			
Resistor RID1 Ω (1%Tolerance)	**Resistor RID0 Ω** (1%Tolerance)	**Address 7'b**	**Address 8'b 0 appended (WRITE)**
0k	0k	0x60	0xC0
0k	3k	0x61	0xC2
0k	11k	0x62	0xC4
0k	100k	0x63	0xC6
3k	0k	0x64	0xC8
3k	3k	0x65	0xCA
3k	11k	0x66	0XCC
3k	100k	0x67	0XCE
11k	0k	0x68	0XD0
11k	3k	0x69	0XD2
11k	11k	0x6A	0XD4
11k	100k	0x6B	0XD6
100k	0k	0x6C	0XD8
100k	3k	0x6D	0XDA
100k	11k	0x6E	0XDC
100k	100k	0x6F	0XDE

Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN) and Output State Select (OSS_SEL)

When PDB is driven HIGH, the Deserializer's CDR PLL begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the DS90UB914Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The states of the outputs are based on the OEN and OSS_SEL setting (Table 5). See Figure 17.

TABLE 9. Output States

Inputs				Outputs			
Serial Inputs	**PDB**	**OEN**	**OSS**	**LOCK**	**Pass**	**DATA, GPIO, I2S**	**CLK**
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/Osc(Register Bit Enable)
Static	1	1	1	H	Previous State	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

Programmable Controller

An integrated I2C slave controller is embedded in the DS90UB913Q Serializer as well as the DS90UB914Q Deserializer. It must be used to configure the extra features embedded within the programmable registers or it can be used to control the set of programmable GPIOs.

Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I²C bus. The DS90UB913/914 provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the SLAVE_ID_MATCH register on Deserializer. This will remap

the SLAVE_ID_MATCH address to the target SLAVE_ID_INDEX address; up to 8 ID indexes are supported. The ECU Controller must keep track of the list of I²C peripherals in order to properly address the target device.

See *Figure 34* for an example of this function.

- ECU is the I²C master and has an I²C master interface
- The I²C interfaces in DES A and DES B are both slave interfaces
- The I²C protocol is bridged from DES A to SER A and from DES B to SER B
- The I²C interfaces in SER A and SER B are both master interfaces

If master controller transmits I²C slave 0xA0, the DES A address 0xC0 will forward the transaction to remote Camera A. If the controller transmits slave address 0xA4, the DES B 0xC2 will recognize that 0xA4 is mapped to 0xA0 and will be transmitted to the remote Camera B. If controller sends command to address 0xA6, the DES B 0xC2 will forward transaction to slave device 0xA2.

The Slave ID index/match is supported only in the camera mode (SER: MODE pin = L; DES: MODE pin = H). For Multiple device addressing in display mode (SER: MODE pin = H; DES: MODE pin = L), use the I²C pass through function.

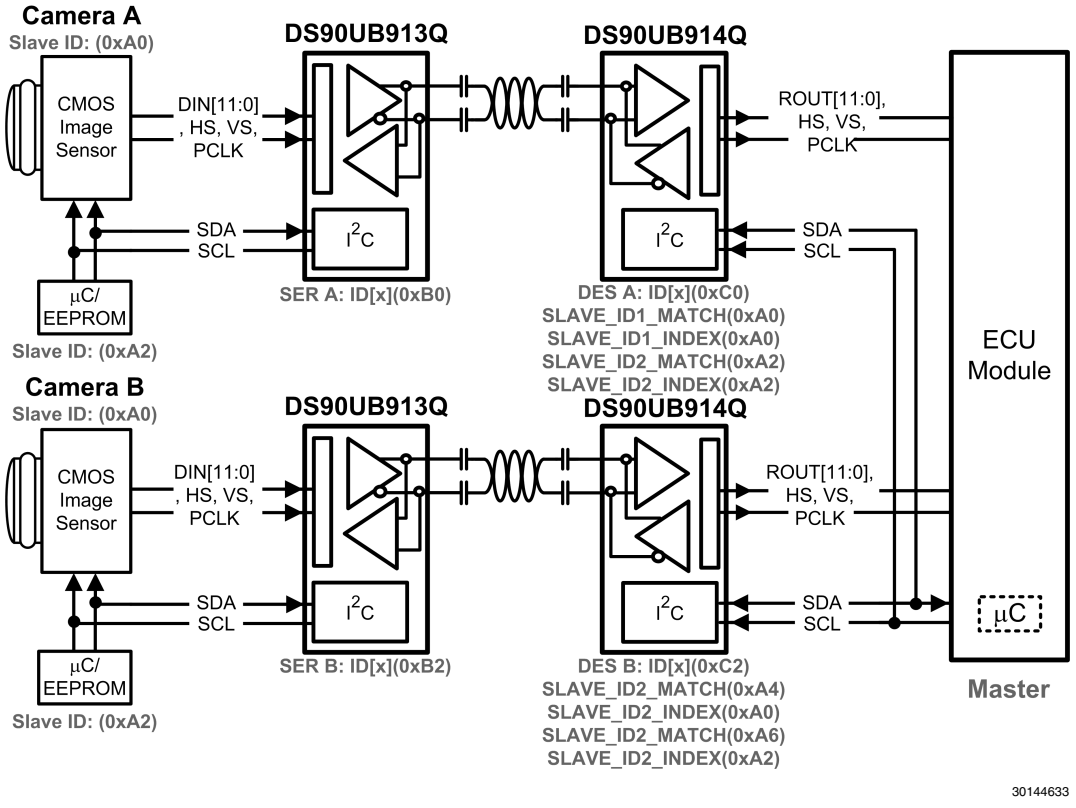


FIGURE 34. Multiple Device Addressing

Synchronizing Multiple Cameras

For applications requiring multiple cameras for frame-synchronization, it is recommended to utilize the General Purpose Input/ Output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller needs to provide a field sync output (such as a vertical or frame sync signal) and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the birectional control channel, there will be a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPIO data transmitted across multiple links is 25µs.

Note: The user must verify that the timing variations between the different links are within their system and timing specifications.

See *Figure 35* for an example of this function.

The maximum time (t1) between the rising edge of GPIO (i.e. sync signal) arriving at Camera A and Camera B is 25µs.

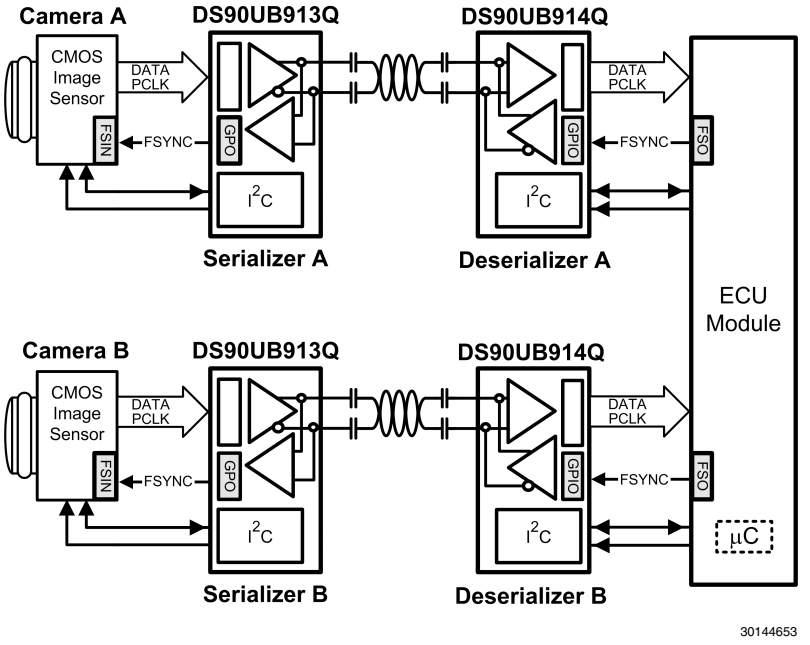


FIGURE 35. Synchronizing Multiple Cameras

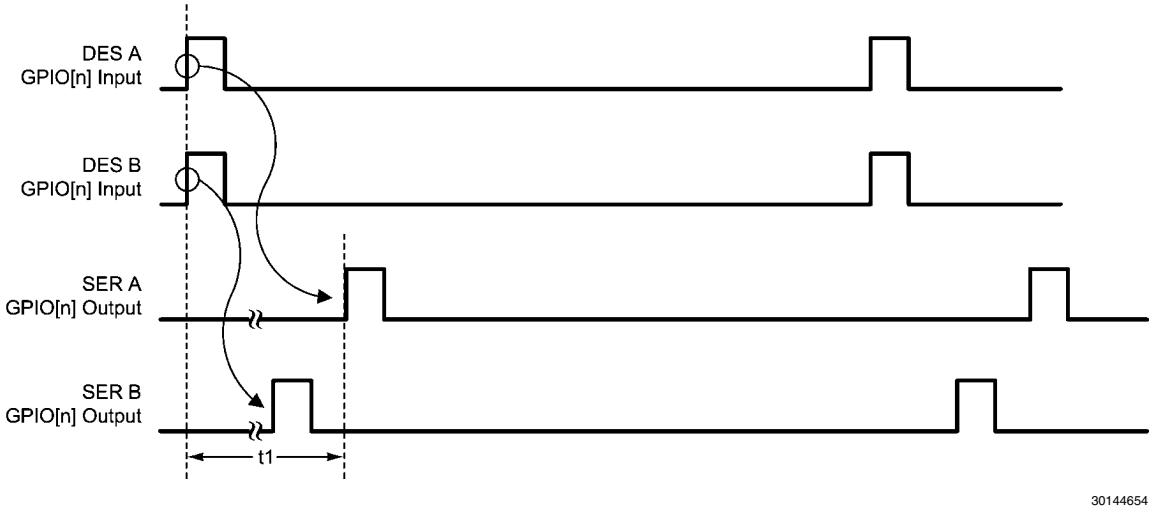


FIGURE 36. GPIO Delta Latency

General Purpose I/O (GPIO) Descriptions

There are 4 GPOs on the Serializer and 4 GPIOs on the Deserializer when the DS90UB913/914Q chipsets are run off the pixel clock from the imager as the reference clock source. The GPOs on the Serializer can be configured as outputs for the input signals that are fed into the Deserializer GPIOs. In addition, the GPOs on the Serializer can behave as outputs of the local register on the Serializer. The GPIOs on the Deserializer can be configured to be the input signals feeding the output of the GPOs on the Serializer. In addition the GPIOs on the Deserializer can be configured to behave as outputs of the local register on the Deserializer. If the DS90UB913/914Q chipsets are run off the external oscillator source as the reference clock, then GPO3 on the Serializer is automatically configured to be the input for the external clock and GPIO2 on the Deserializer is configured to be the output of the divide-by-2 clock which is fed into the imager as its reference clock. In this case, the GPIO2 and GPIO3 on the Deserializer can only behave as outputs of the local register on the Deserializer. The GPIO maximum switching rate is up to 66 kHz when configured for communication between Deserializer GPIO to Serializer GPO.

LVCMOS VDDIO Option

1.8V/2.8V/3.3V Serializer inputs and 1.8V/3.3V Deserializer outputs are user configurable to provide compatibility with 1.8V, 2.8V and 3.3V system interfaces.

Deserializer – Adaptive Input Equalization(AEQ)

The receiver inputs provide an adaptive input equalization filter in order to compensate for loss from the media. The level of equalization can also be manually selected via register controls. The fully adaptive equalizer output can be seen using the CMLOUTP/CMLOUTN pins in the Deserializer.

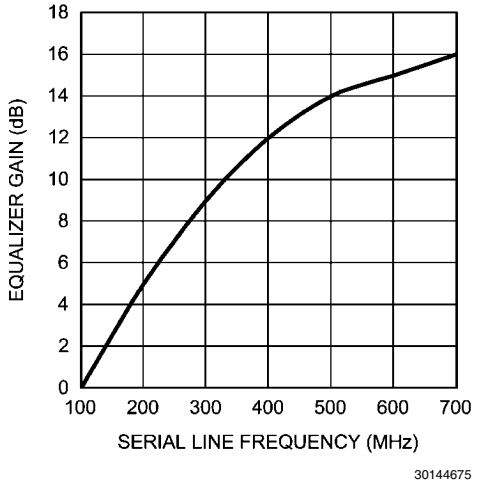


FIGURE 37. Maximum Equalizer Gain vs. Line Frequency

EMI Reduction

Deserializer Staggered Output

The receiver staggers output switching to provide a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

Spread Spectrum Clock Generation(SSCG) on the Deserializer

The DS90UB914Q parallel data and clock outputs have programmable SSCG ranges from 10 MHz to 100 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers on the DS90UB914Q device. SSC profiles can be generated using bits [3:0] in register 0x02 in the Deserializer.

Powerdown

The SER has a PDB input pin to ENABLE or Powerdown (SLEEP) the device. The modes can be controlled by the host and is used to disable the Link to save power when the remote device is not operational. In this mode, if the PDB pin is tied High and the SER will enter SLEEP when the PCLK stops. When the PCLK starts again, the SER will then lock to the valid input PCLK and transmit the data to the DES. In SLEEP mode, the high-speed driver outputs are static (High). The DES has a PDB input pin to ENABLE or Powerdown (SLEEP) the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied High and the DES will enter SLEEP when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In SLEEP mode, the Data and PCLK outputs are set by the OSS_SEL configuration.

Pixel Clock Edge Select (TRFB / RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the falling edge of the PCLK.

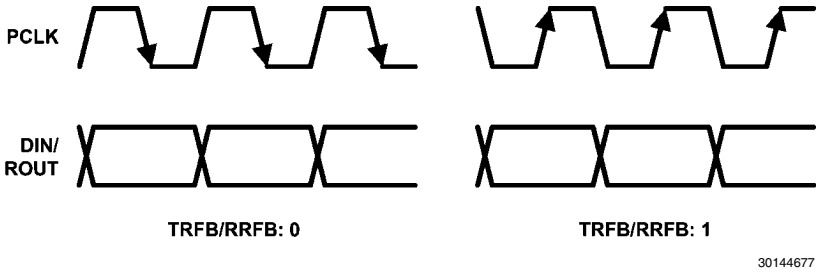


FIGURE 38. Programmable PCLK Strobe Select

Power Up Requirements and PDB Pin

It is required to delay and release the PDB Signal after VDD (VDDn and VDDIO) power supplies have settled to the recommended operating voltage. An external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD has stabilized.

Built In Self Test

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

BIST Configuration and Status

The chipset can be programmed into BIST mode using either pins or registers. By default BIST configuration is controlled through pins. BIST can be configured via registers using BIST Control register (0x24). Pin based configuration is defined as follows:

- BISTEN : Enable the BIST Process
- GPIO0 and GPIO1 : Defines the BIST clock source (PCLK vs. various frequencies of internal OSC

TABLE 10. BIST Configuration

Deserializer GPIO[0:1]	Oscillator Source	BIST Frequency (MHz)
00	External PCLK	PCLK or External Oscillator
01	Internal	50
10	Internal	25
11	Internal	12.5

The BIST mode provides various options for source PCLK. Using external pins, GPIO0 and GPIO1 or using registers, customer can program the BIST mode to use external PCLK or various OSC frequencies. The BIST status can be monitored real time on PASS pin. For every frame with error(s), PASS pin toggles low for half PCLK period. If two consecutive frames have errors, PCLK will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status of the last BIST run. The status can also be read through I2C for the number of frames in errors. BIST status on PASS pin remains until it is changed by a new BIST session or a reset. The BIST status on PASS pin is not maintained till RX loses LOCK after BISTEN is de-assserted. To evaluate BIST in the external oscillator mode, both external oscillator and PCLK need to be present.

The BIST status on PASS pin is not maintained till RX loses LOCK after BISTEN is de-assserted. So for all practical purposes, the BIST status can be monitored from register 0x25 i.e. BIST Error Count on the DS90UB914 Deserializer. To evaluate BIST in the external oscillator mode, both external oscillator and PCLK need to be present.

Sample BIST Sequence

Step1. For the DS90UB913/914Q FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UB914Q FPD-Link III deserializer. The desired clock source is selected through the GPIO0 and GPIO1 pins as shown in Table 6.

Step2. The DS90UB913Q Serializer is woken up through the back channel if it is not already on. The SSO pattern on the data pins is send through the FPD-Link III to the deserializer. Once the serializer and deserializer are in the BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking data stream. If an error in the payload is detected the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step3. To stop the BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data. The final test result is not maintained on the PASS pin. To monitor the BIST status, check the BIST Error Count register, 0x25 on the Deserializer.

Step4. The link returns to normal operation after the deserailzer BISTEN pin is low. *Figure 40* shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to

generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or by reducing signal condition enhancements (Rx equalization).

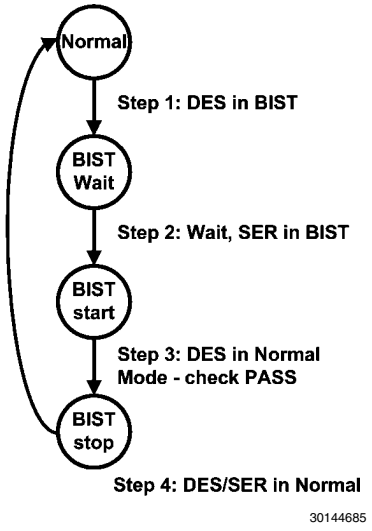


FIGURE 39. AT-Speed BIST System Flow Diagram

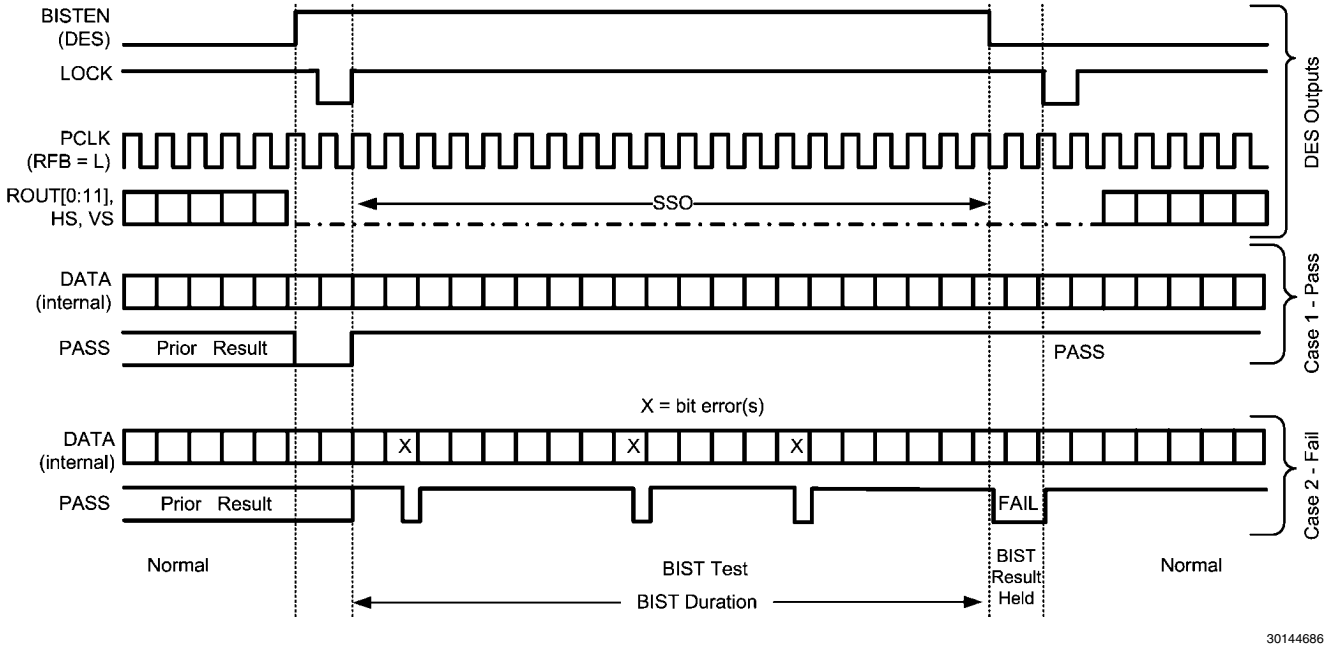


FIGURE 40. BIST Timing Diagram

Applications Information

AC COUPLING

The SER/DES supports only AC-coupled interconnects through an integrated DC balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in *Figure 41*.

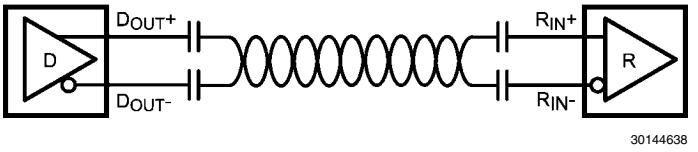


FIGURE 41. AC-Coupled Connection

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/O's require a 100 nF AC coupling capacitors to the line.

Adaptive Equalizer – Loss Compensation

The adaptive equalizer is designed to compensate for signal degradation due to the differential insertion loss of the interconnect components. There are limits to the amount of loss that can be compensated – these limits are defined by the gain curve of the equalizer. In addition, there is an inherent tolerance for loss defined by the delta between the serializer's minimum VOD and the input threshold (Vswing) of the deserializer. In order to determine the maximum cable reach, other factors that affect signal integrity such as jitter, skew, ISI, crosstalk, etc. need to be taken into consideration. *Figure 42* illustrates the maximum allowable interconnect loss with the adaptive equalizer at its maximum gain setting ("914 equalizer gain").

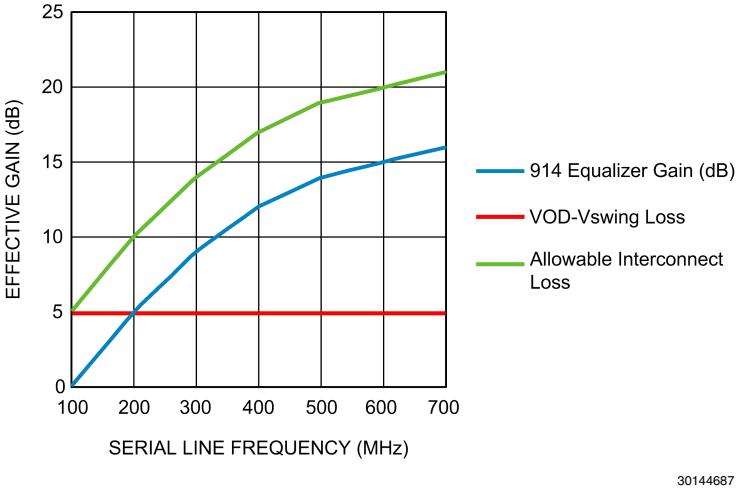


FIGURE 42. Adaptive Equalizer – Interconnect Loss Compensation

Figure 43 shows the typical connection of a DS90UB913Q Serializer

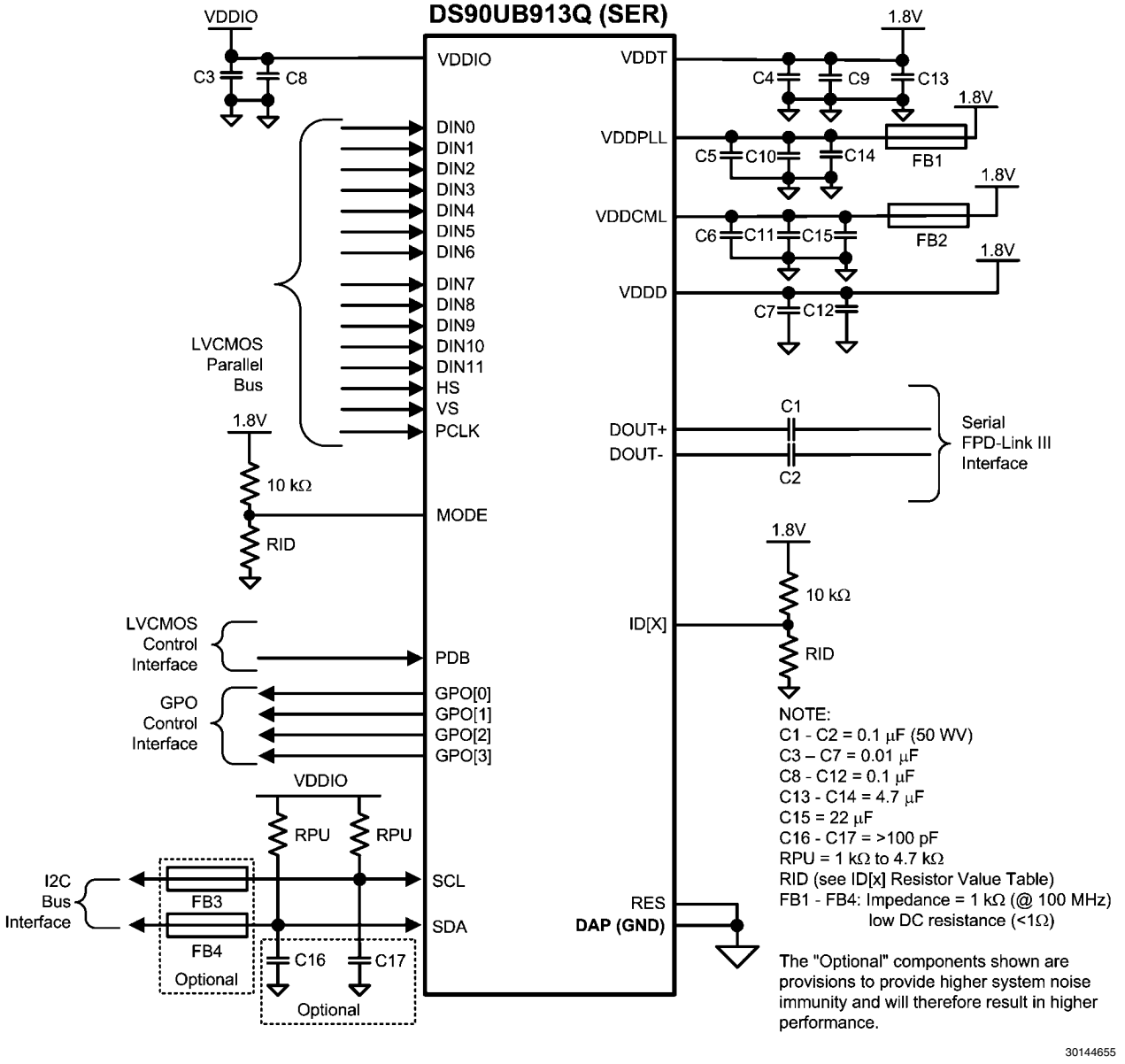


FIGURE 43. DS90UB913Q Typical Connection Diagram — Pin Control

Figure 44 shows a typical connection of the DS90UB914Q Deserializer.

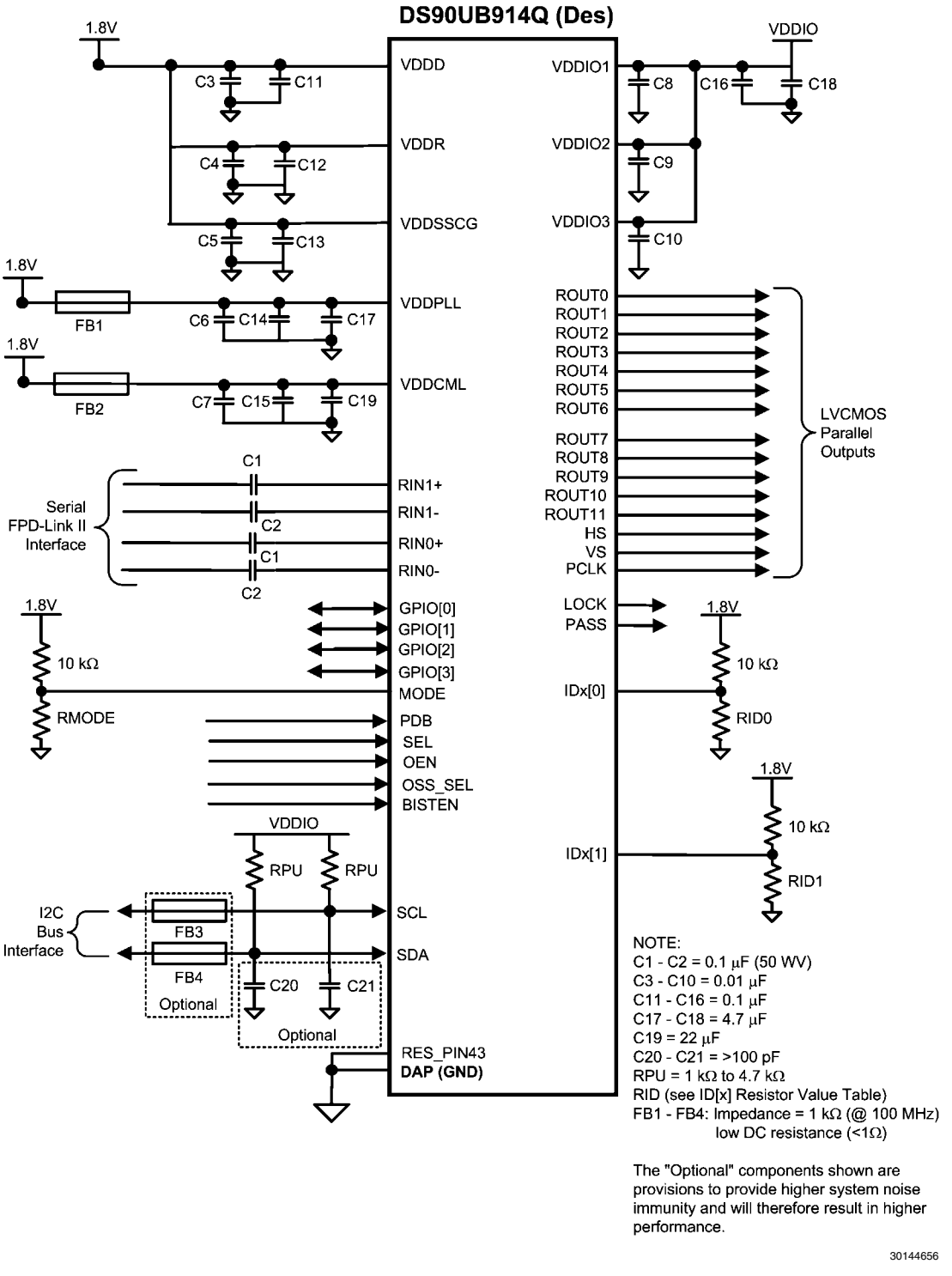


FIGURE 44. DS90UB914Q Typical Connection Diagram — Pin Control

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ohms are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in Ti's Application Note: AN-1187/SN0A401Q.

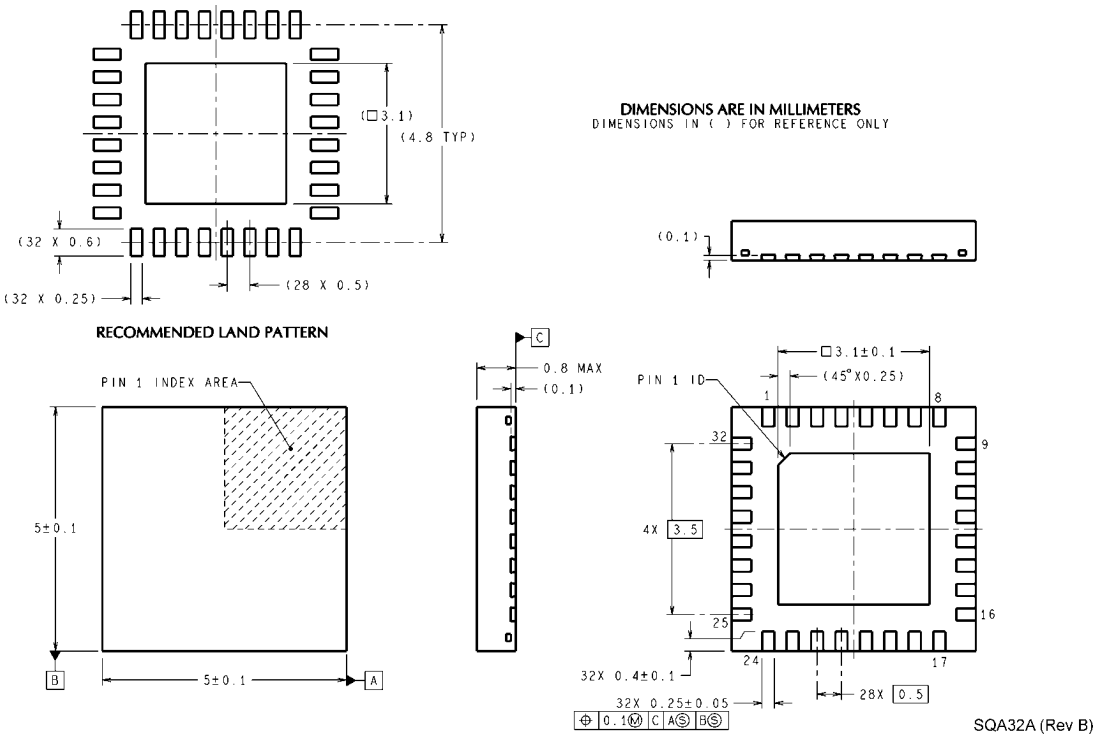
INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

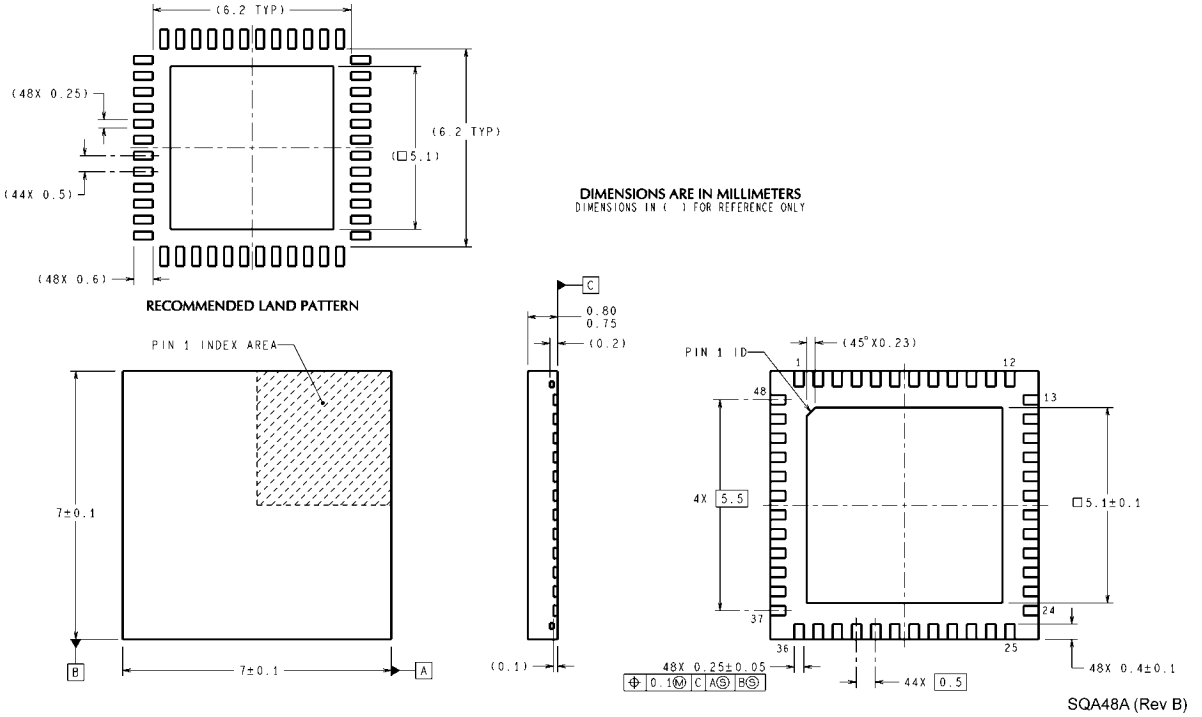
- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  – S = space between the pair
  – 2S = space between pairs
  – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: **www.ti.com/lvds**

Physical Dimensions inches (millimeters) unless otherwise noted



DS90UB913Q SQ
Package Number SQA32A



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Notes

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